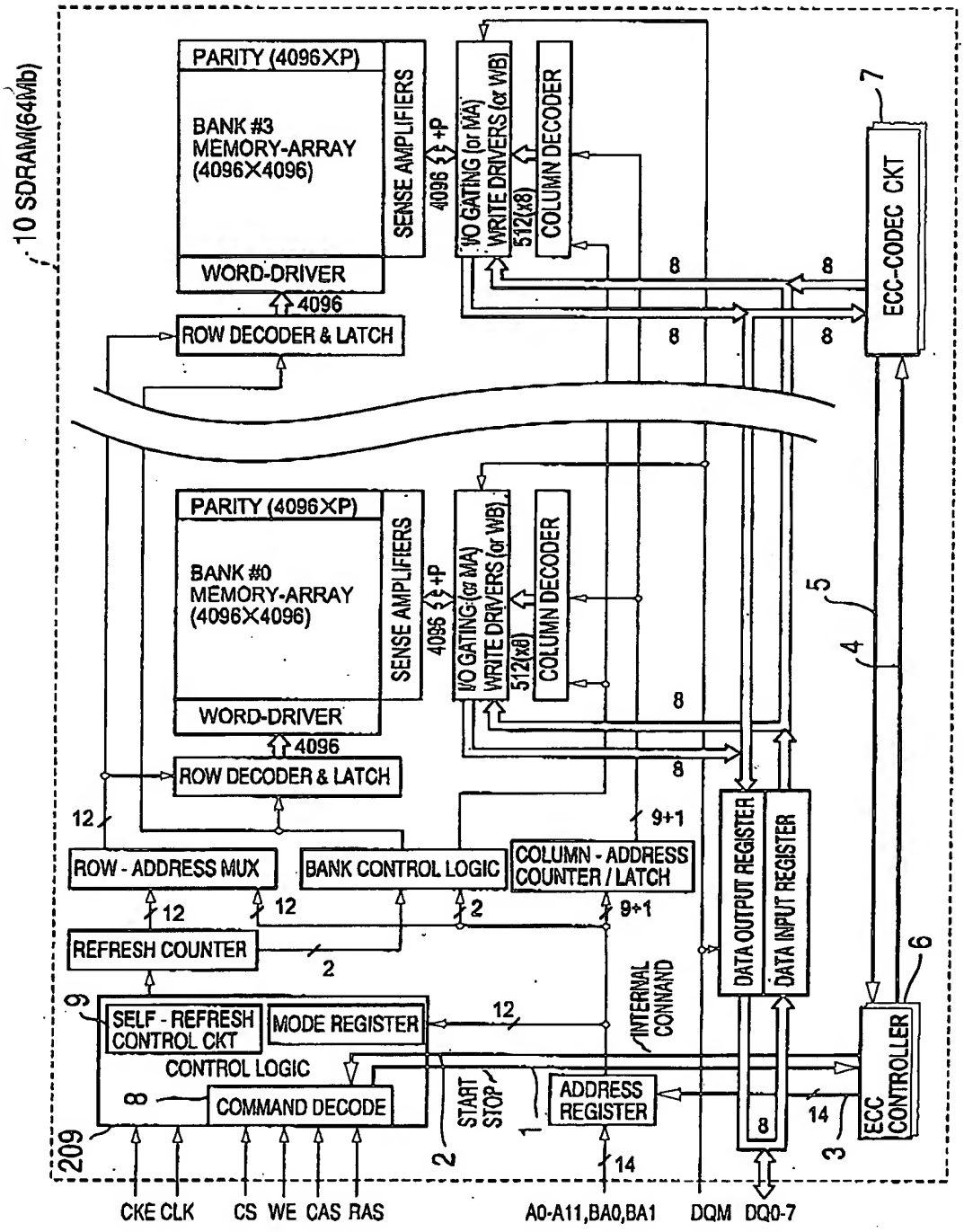
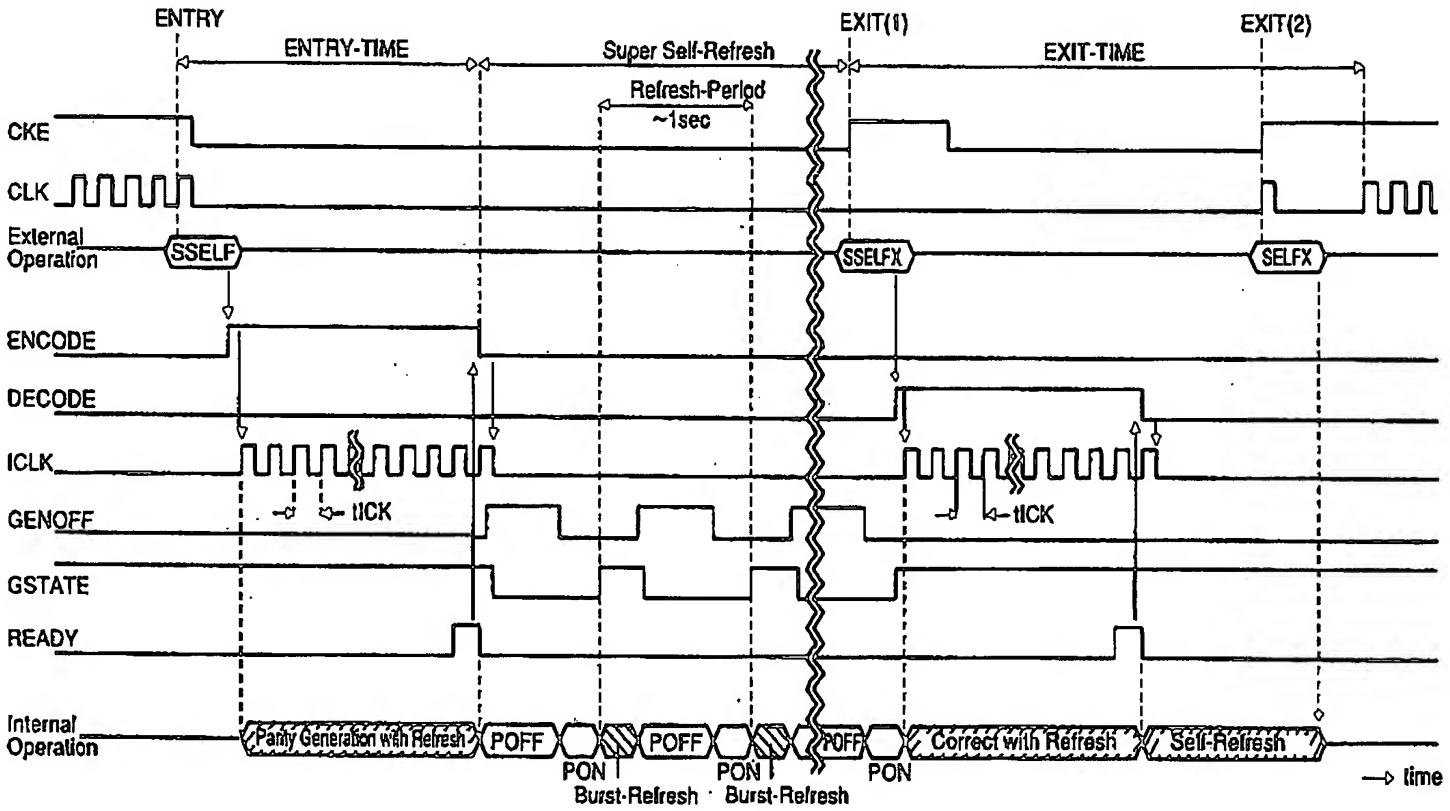

10 SDRAM(64Mb)
PARITY (4096XP)
BANK #3
MEMORY-ARRAY
(4096X4096)
WORD-DRIVER
4096
ROW DECODER & LATCH
SENSE AMPLIFIERS
4096 +P
I/O GATING (or MA)
WRITE DRIVERS (or WB)
512(x8)
COLUMN DECODER
8
ECC-CODEC CKT
7
PARITY (4096XP)
BANK #0
MEMORY-ARRAY
(4096X4096)
WORD-DRIVER
4096
ROW DECODER & LATCH
SENSE AMPLIFIERS
4096 +P
I/O GATING (or MA)
WRITE DRIVERS (or WB)
512(x8)
COLUMN DECODER
8
5
4
12
9+1
ROW - ADDRESS MUX
BANK CONTROL LOGIC
COLUMN - ADDRESS COUNTER / LATCH
12
12
2
9+1
REFRESH COUNTER
2
DATA OUTPUT REGISTER
DATA INPUT REGISTER
6
9
SELF - REFRESH CONTROL CKT
MODE REGISTER
12
INTERNAL COMMAND
CONTROL LOGIC
8
COMMAND DECODE
START STOP
2
1
ADDRESS REGISTER
14
8
14
3
ECC CONTROLLER
209
CKE CLK
CS WE CAS RAS
A0-A11,BA0,BA1
DQM
DQ0-7

FIG. 1




Sequence of Super Self-Refresh Operation (Entry/Exit Scheme)

FIG. 2

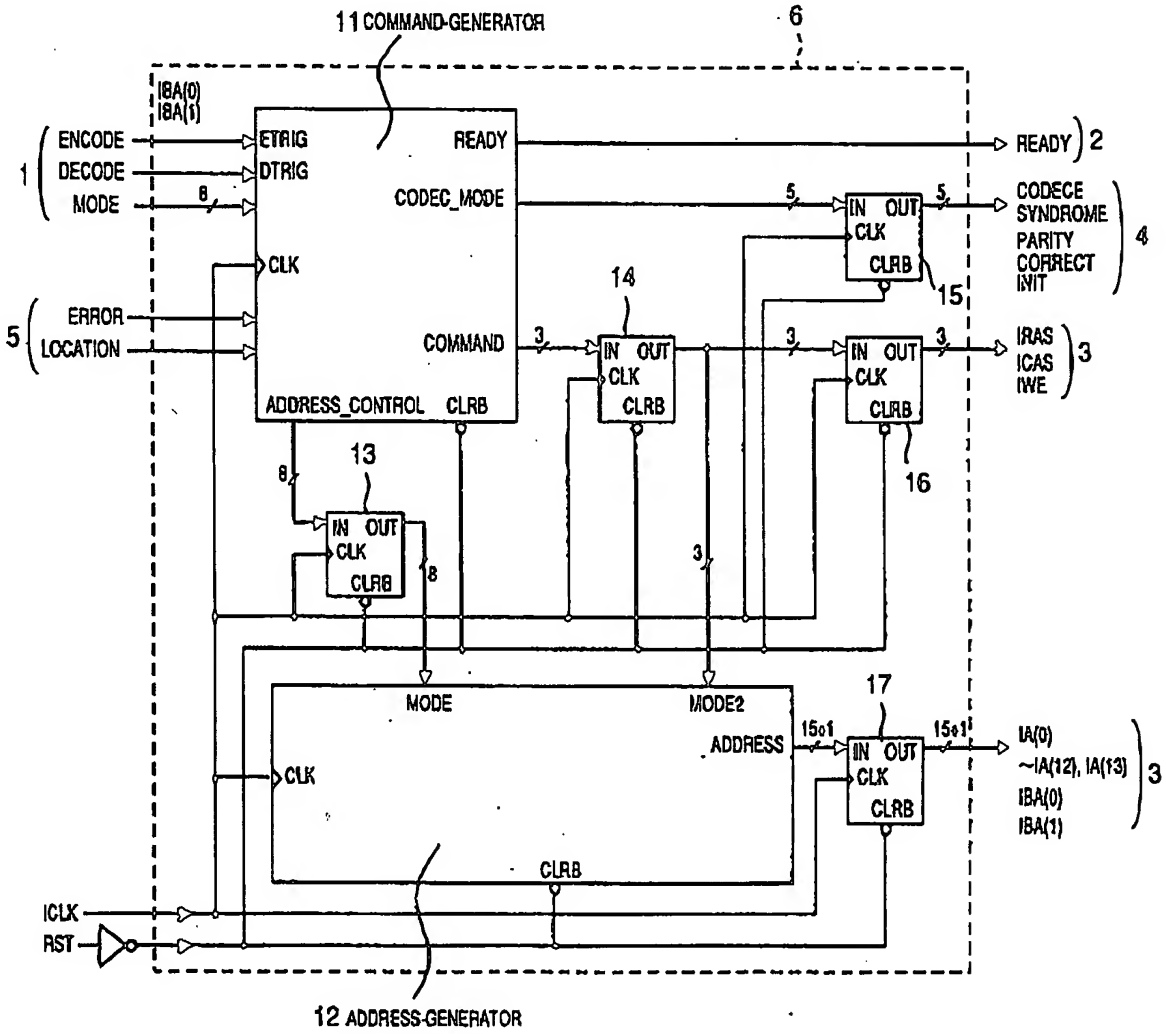

11 COMMAND-GENERATOR
6
IBA(0)
IBA(1)
ENCODE
DECODE
MODE
1
ETRIG
DTRIG
CLK
ERROR
LOCATION
5
READY
CODEC_MODE
COMMAND
ADDRESS_CONTROL
CLRB
READY 2
CODECE
SYNDROME
PARITY
CORRECT
INIT
4
IRAS
ICAS
IWE
3
IN OUT
CLK
CLRB
13
14
15
16
17
MODE
MODE2
ADDRESS
IA(0)
~IA(12), IA(13)
IBA(0)
IBA(1)
3
ICLK
RST
12 ADDRESS-GENERATOR

FIG. 3

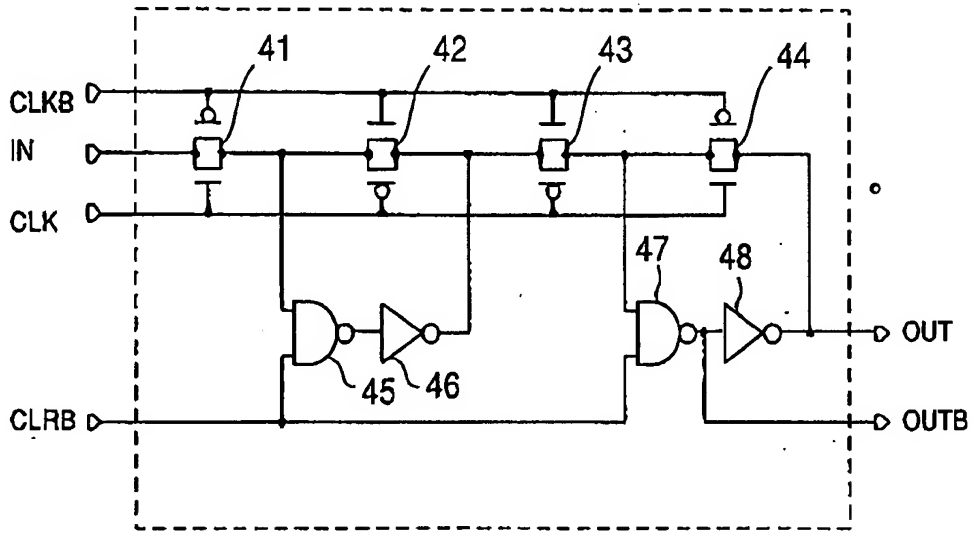

41
42
43
44
CLKB
IN
CLK
47
48
OUT
45
46
CLRB
OUTB

FIG. 4B

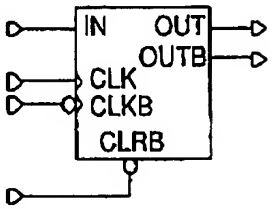

IN
OUT
OUTB
CLK
CLKB
CLRB

FIG. 4A

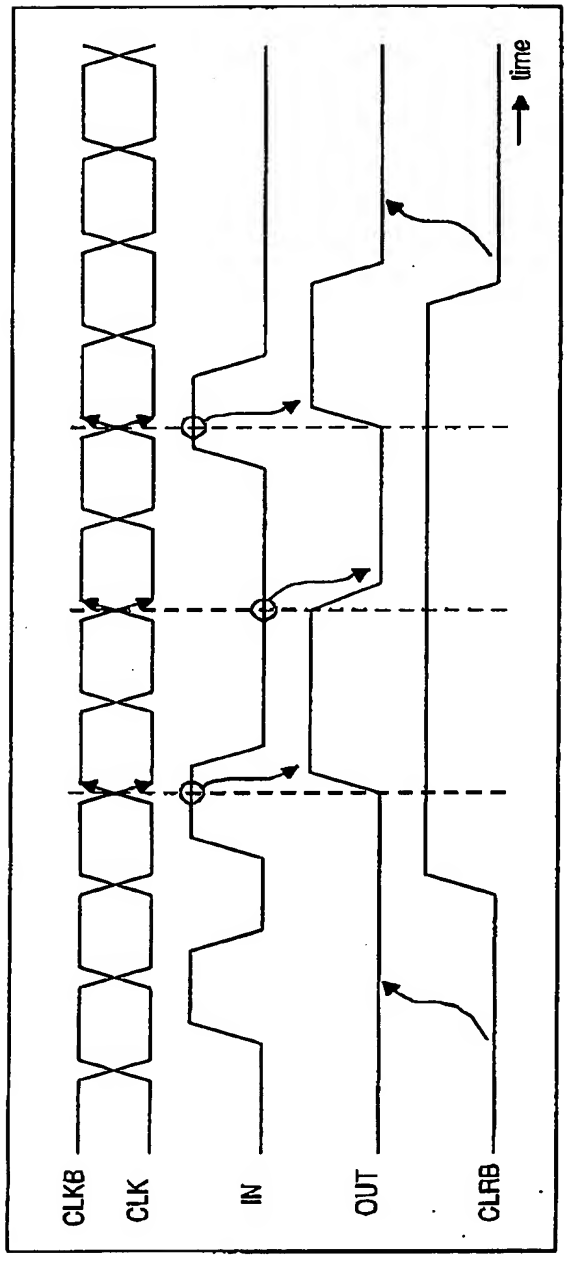



FIG. 5

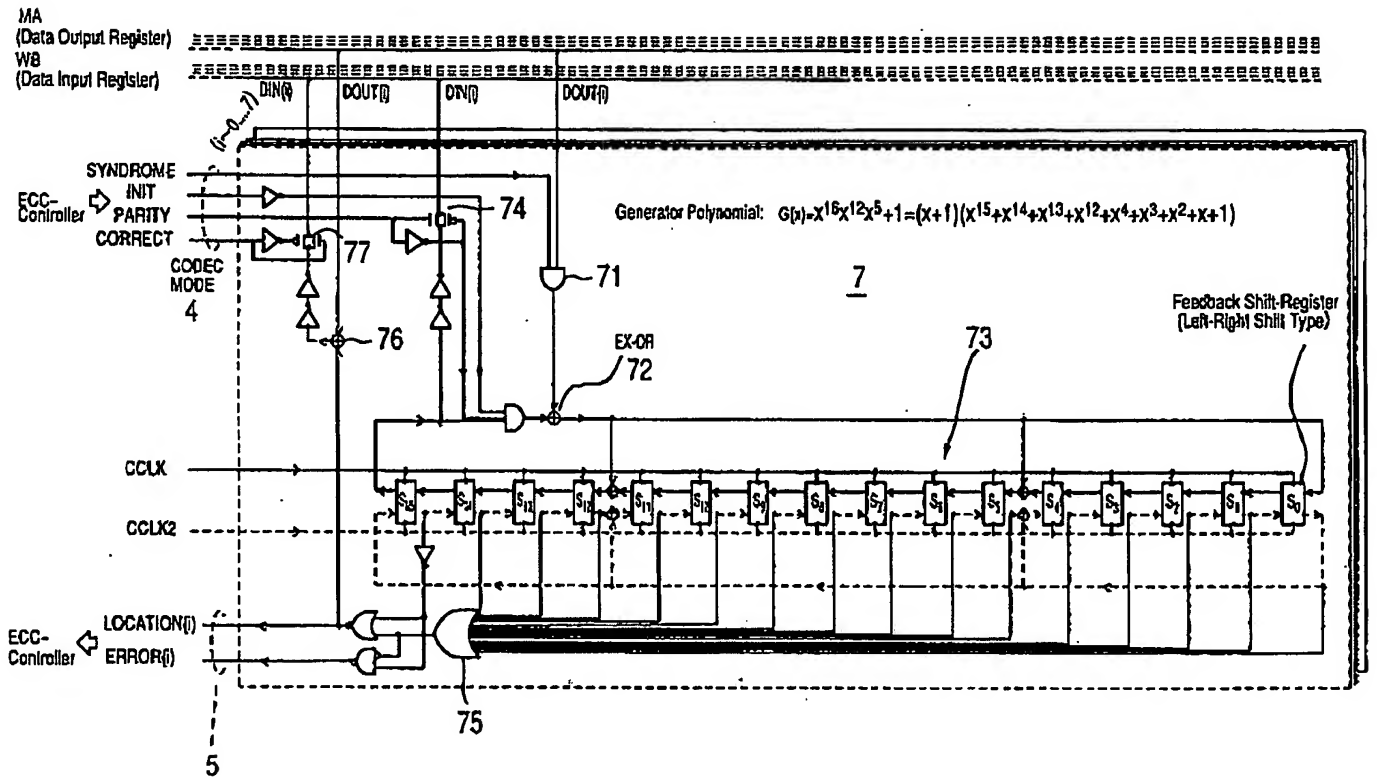
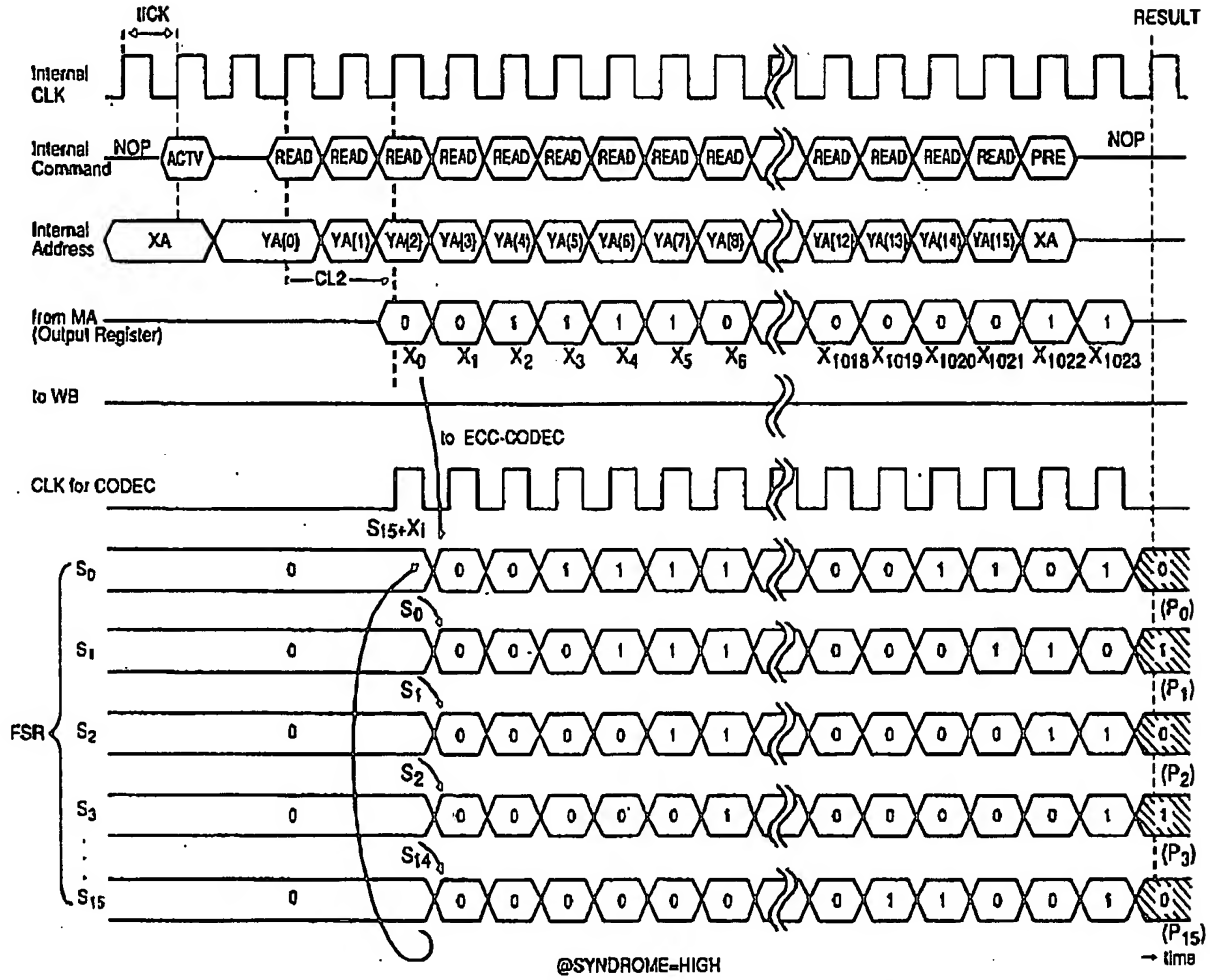
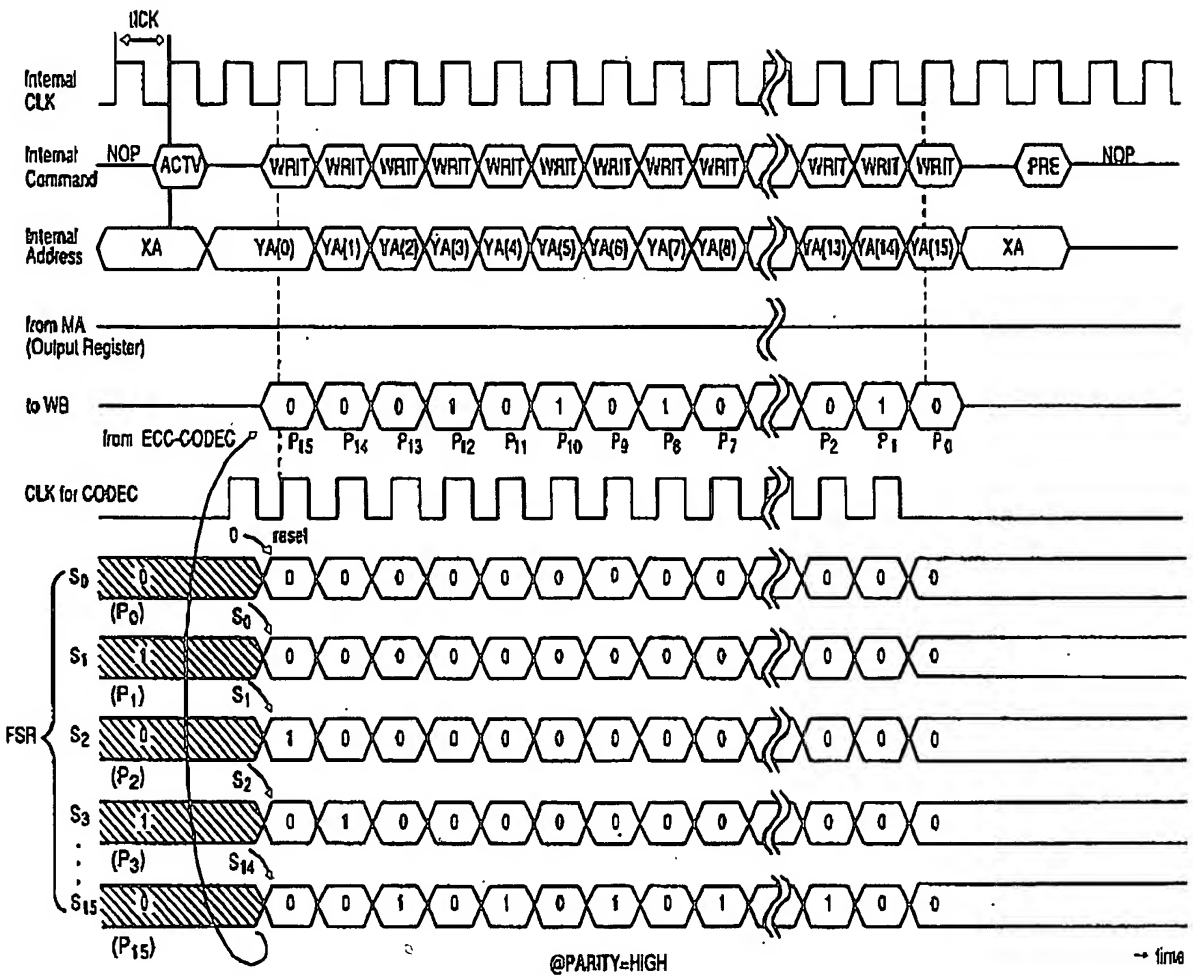

MA
(Data Output Register)
WB
(Data Input Register)
DIN(i)
DOUT(i)
DIN(i)
DOUT(i)
(i=0,...7)
SYNDROME
INIT
ECC-Controller
PARITY
CORRECT
CODEC MODE
4
74
77
71
7
Generator Polynomial: G(x)=X16X12X5+1=(X+1)(X15+X14+X13+X12+X4+X3+X2+X+1)
Feedback Shift-Register (Left-Right Shift Type)
76
EX-OR
72
73
CCLK
CCLK2
LOCATION(i)
ECC-Controller
ERROR(i)
75
5

FIG. 6



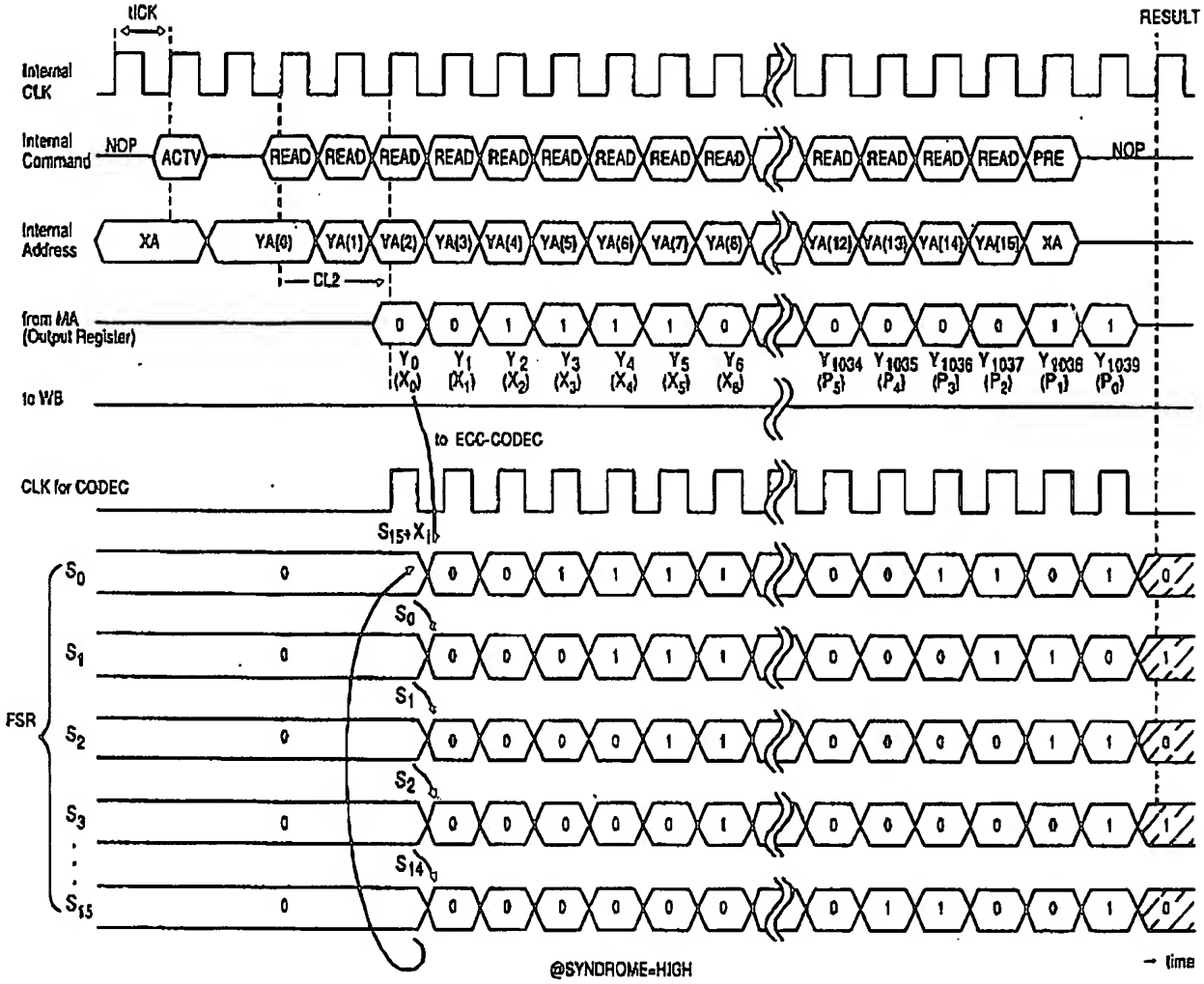

Example 1 of Super Self-Refresh Internal Operation
(Parity-Generation (1) Parity Bit Calculation)

FIG. 7



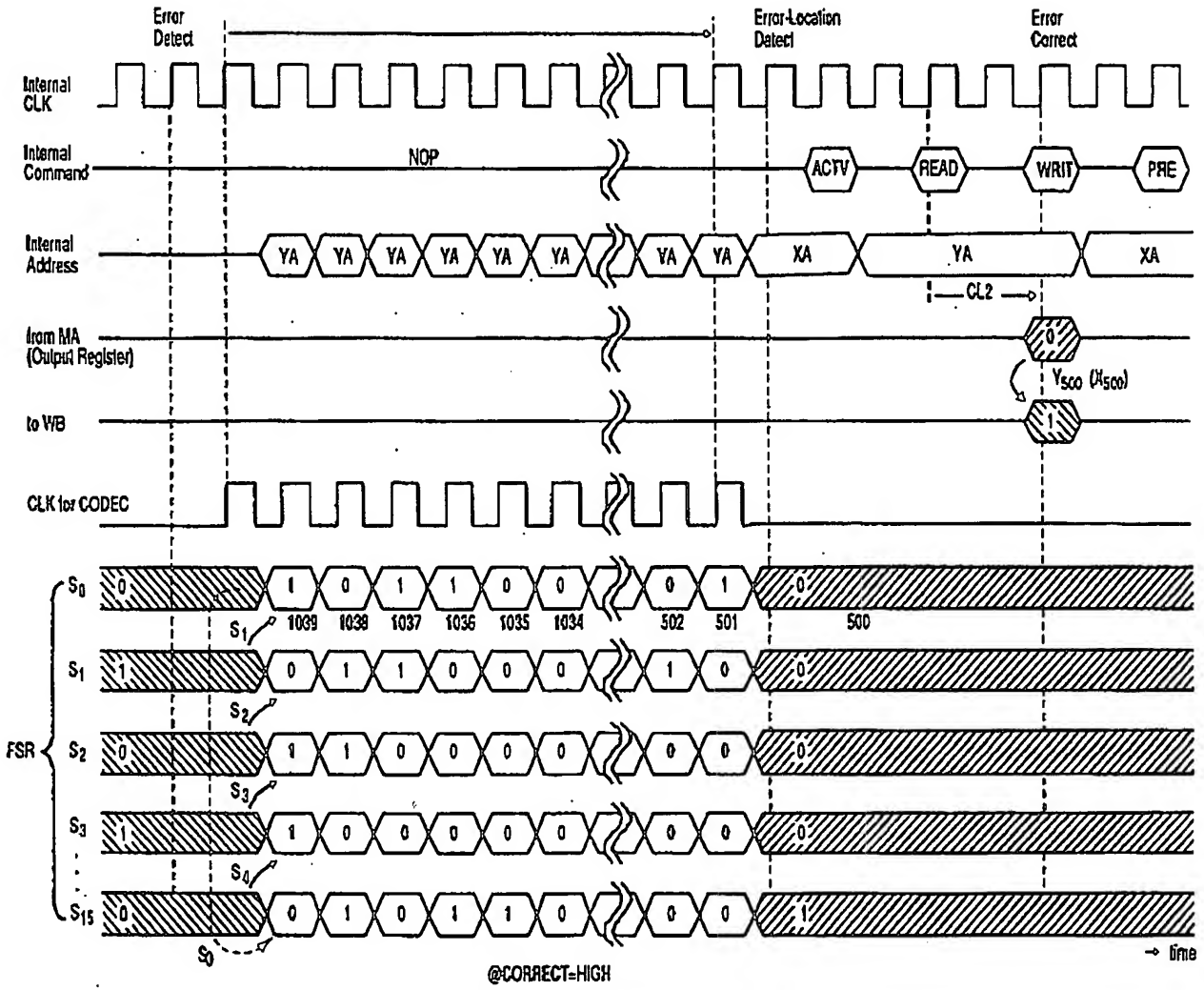

Example 1 of Super Self-Refresh Internal Operation
(Parity-Generation (2) Parity Bit Writing)

FIG. 8




Example 2 of Super Self-Refresh Internal Operation
(Correct (1) Syndrome Calculation)

FIG. 9




Example 2 of Super Self-Refresh Internal Operation
(Correct (2) Error Location Detection and Correction/Writing)

FIG. 10

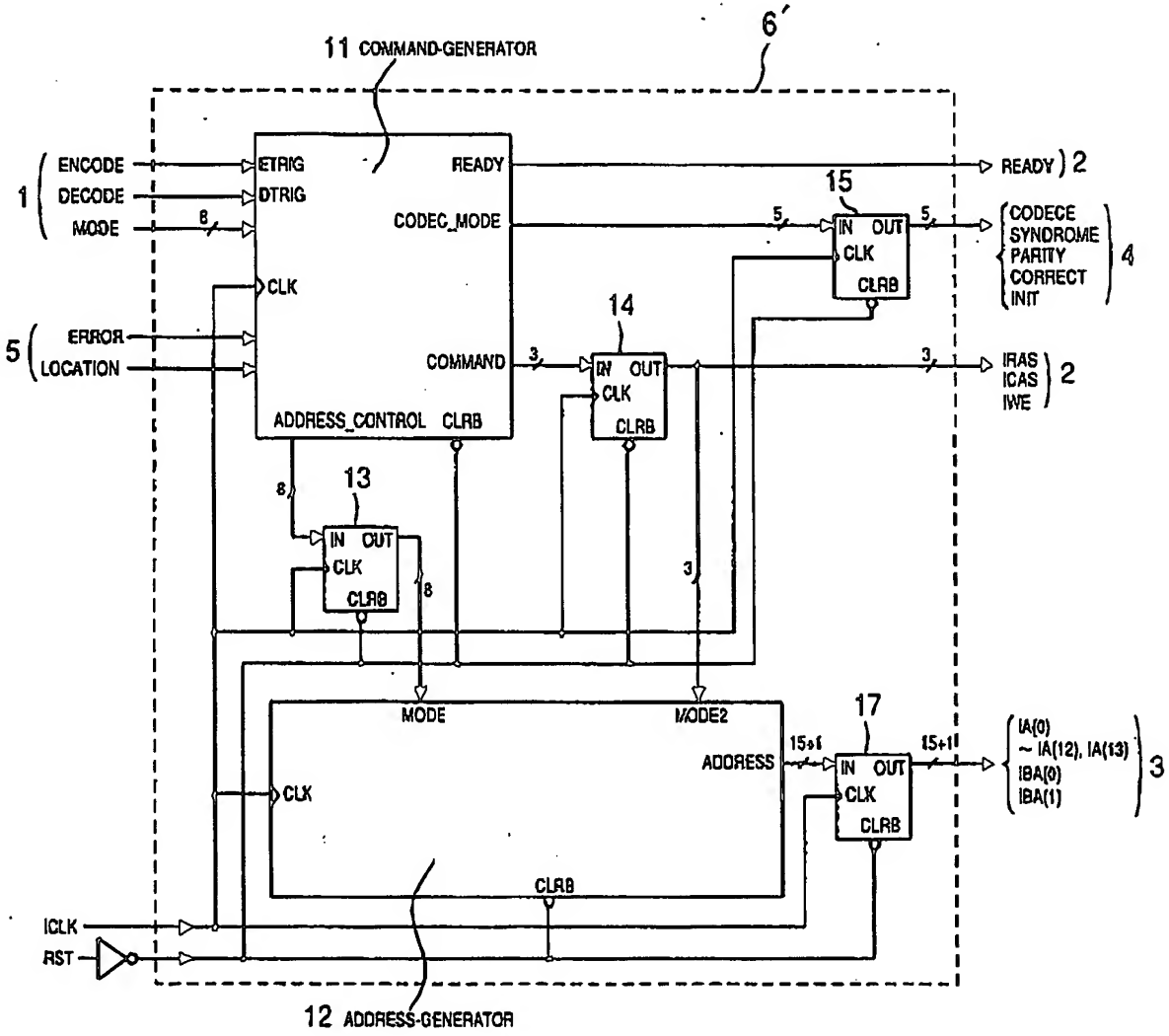

6'
11 COMMAND-GENERATOR
1
ENCODE
DECODE
MODE
8
ETRIG
DTRIG
CLK
READY
CODEC_MODE
COMMAND
ADDRESS_CONTROL
CLRB
READY
2
15
IN
OUT
CLK
CLRB
5
CODECE
SYNDROME
PARITY
CORRECT
INIT
4
5
ERROR
LOCATION
14
3
IRAS
ICAS
IWE
2
13
8
IN
OUT
CLK
CLRB
MODE
MODE2
17
ADDRESS
15+1
IA(0)
~ IA(12), IA(13)
IBA(0)
IBA(1)
3
ICLK
RST
12 ADDRESS-GENERATOR

FIG. 11

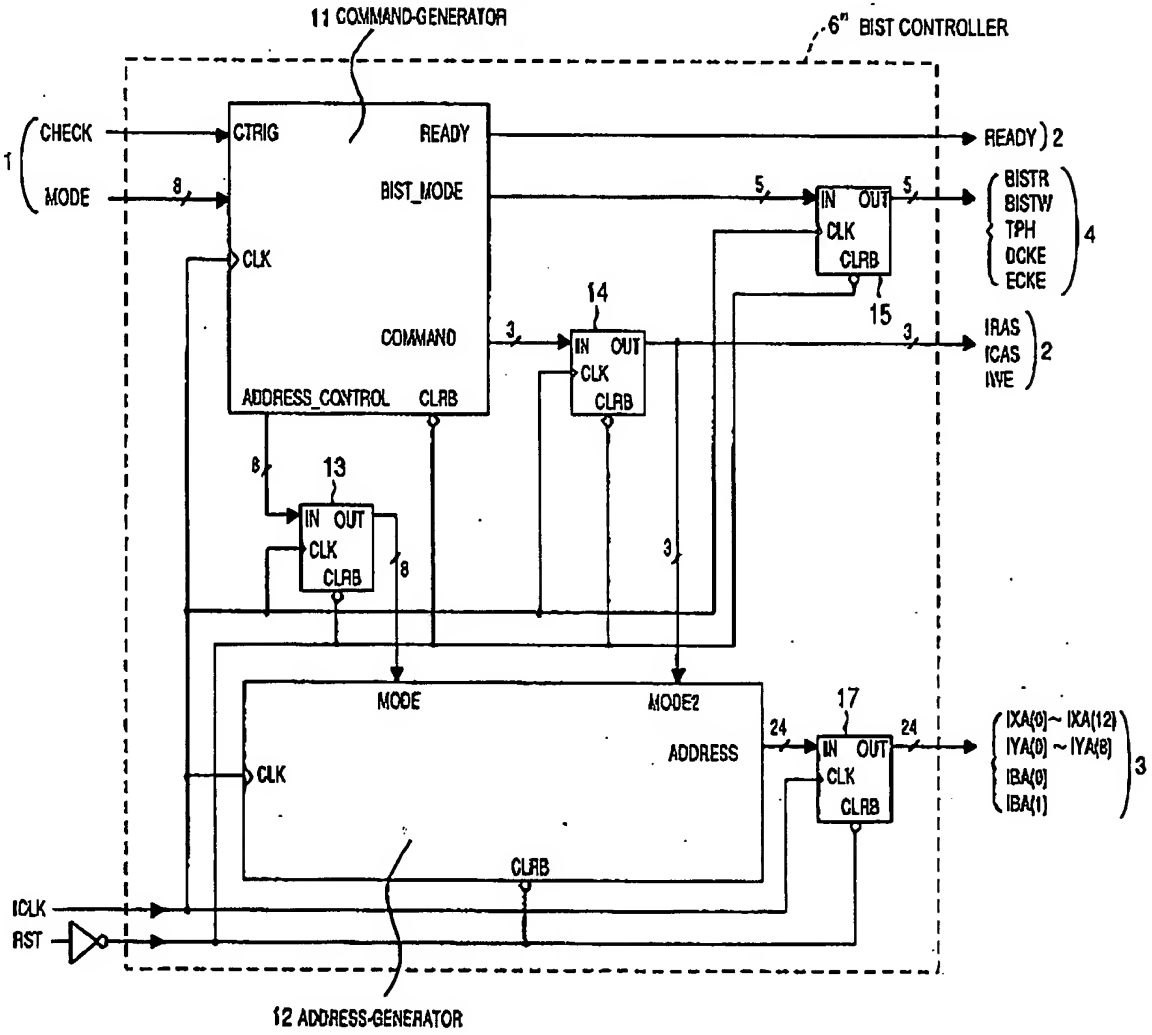
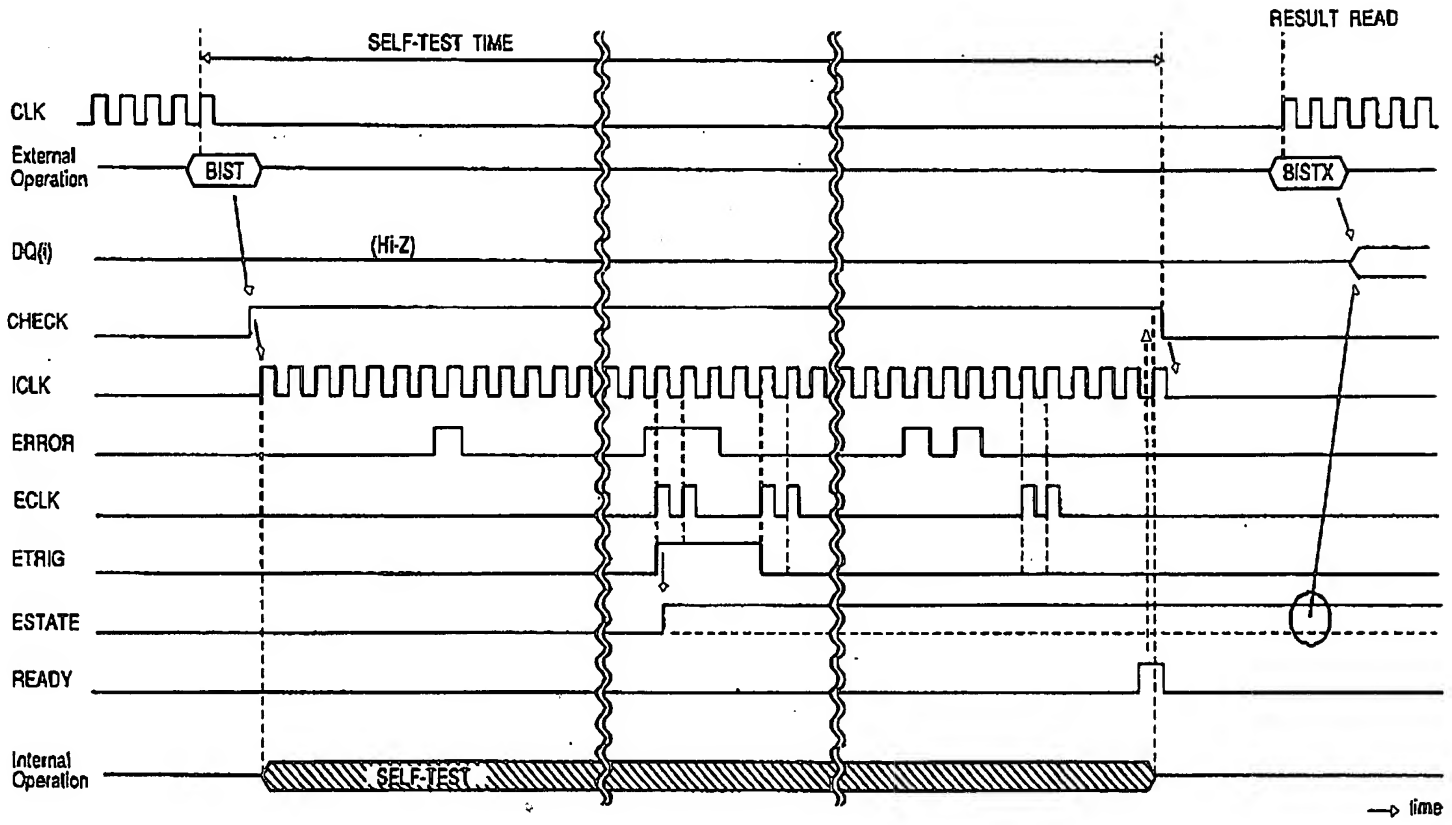

11 COMMAND-GENERATOR
6" BIST CONTROLLER
CHECK
MODE
1
8
CTRIG
READY
BIST_MODE
CLK
COMMAND
ADDRESS_CONTROL
CLRB
READY
2
5
IN OUT
CLK
CLRB
5
BISTR
BISTW
TPH
DCKE
ECKE
4
15
14
3
IN OUT
CLK
CLRB
3
IRAS
ICAS
IWE
2
8
13
IN OUT
CLK
CLRB
8
3
MODE
MODE2
ADDRESS
CLK
CLRB
24
17
IN OUT
CLK
CLRB
24
IXA(0)~ IXA(12)
IYA(0) ~ IYA(8)
IBA(0)
IBA(1)
3
ICLK
RST
12 ADDRESS-GENERATOR

FIG. 12




Operation Sequence of BIST

FIG. 13

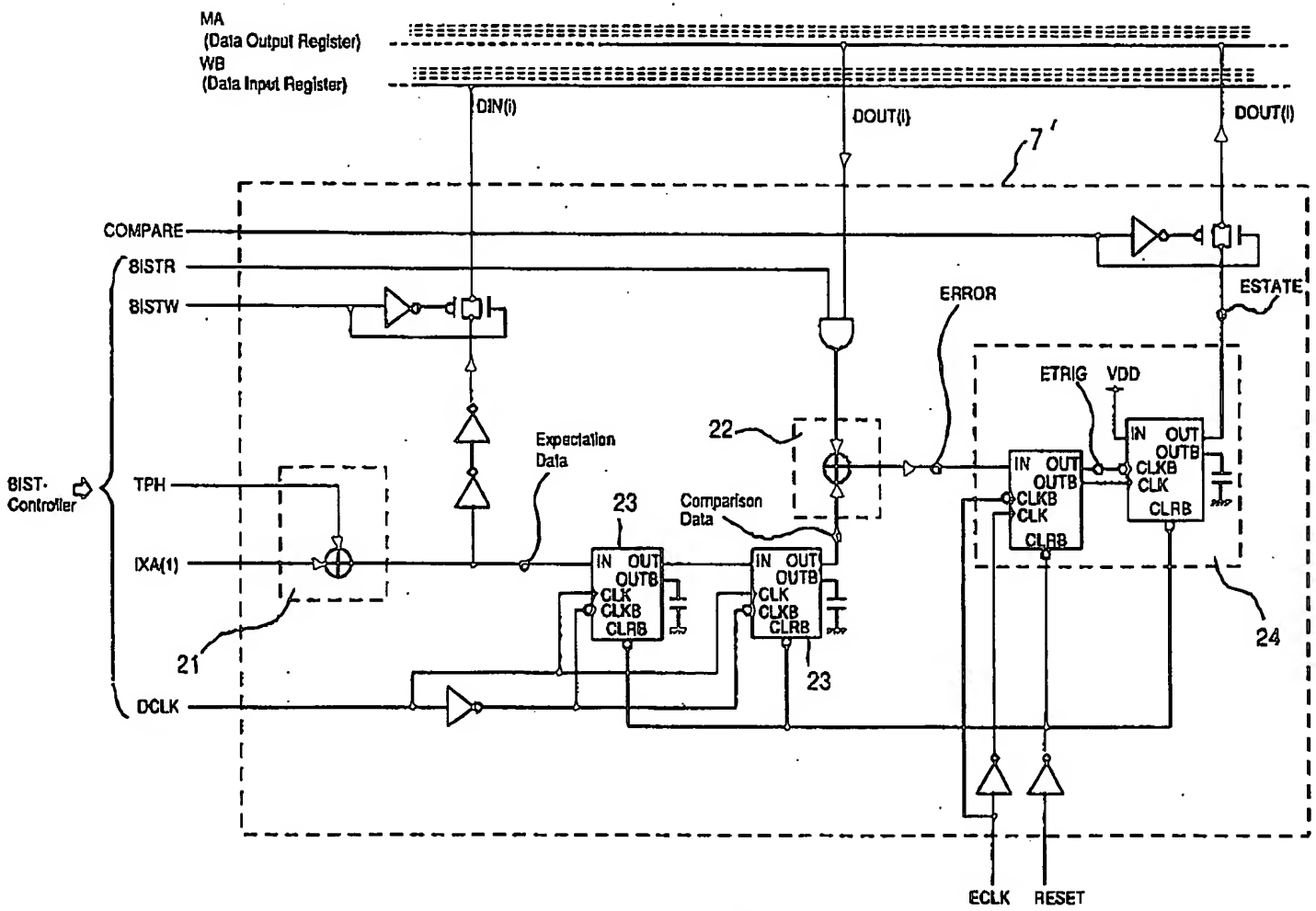

MA
(Data Output Register)
WB
(Data Input Register)
DIN(i)
DOUT(i)
DOUT(i)
7'
COMPARE
BISTR
BISTW
ERROR
ESTATE
ETRIG
VDD
22
Expectation
Data
BIST-
Controller
TPH
IXA(1)
23
Comparison
Data
IN OUT
OUTB
CLK
CLKB
CLRB
21
23
24
DCLK
ECLK
RESET

FIG. 14

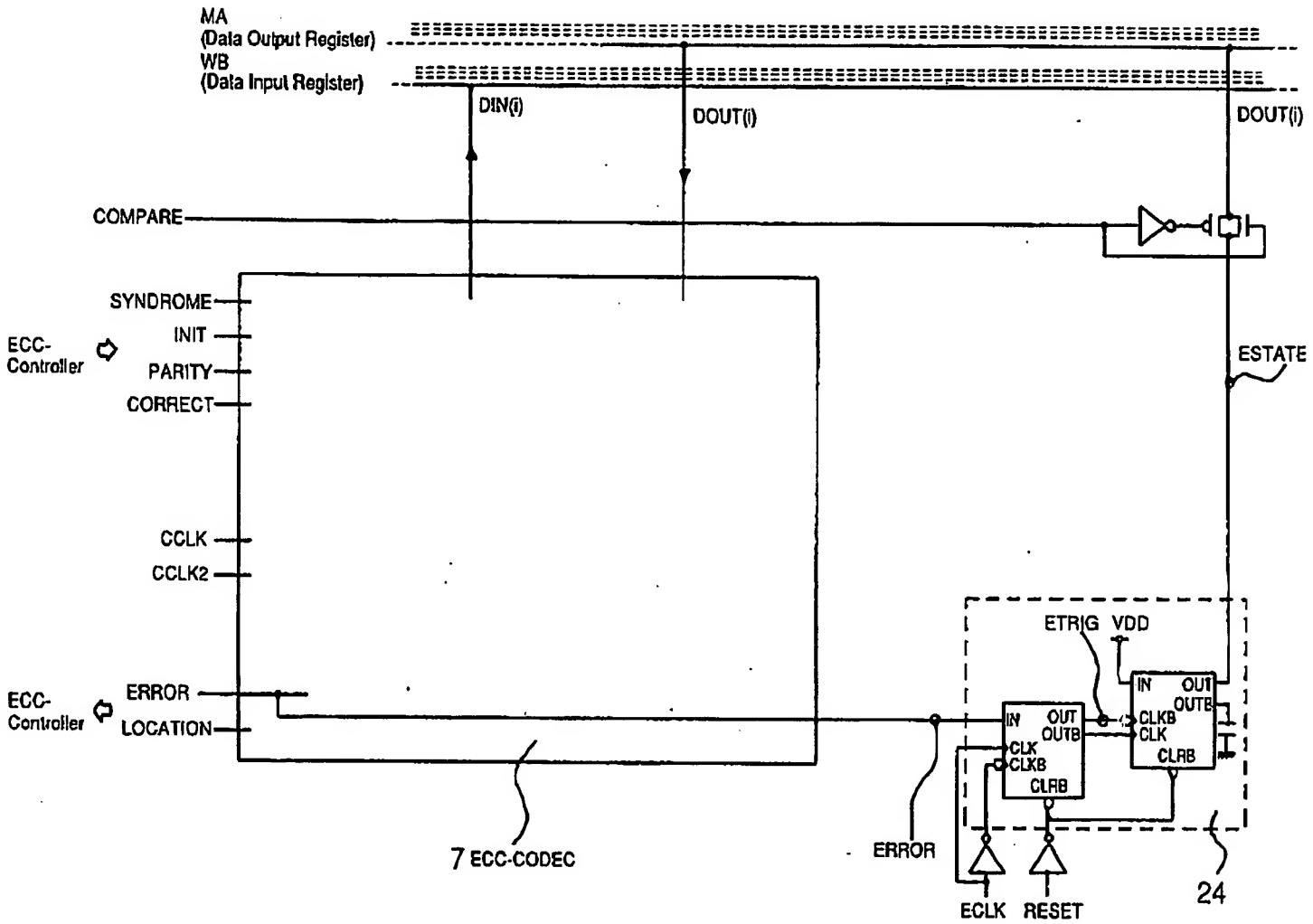

MA
(Data Output Register)
WB
(Data Input Register)
DIN(i)
DOUT(i)
DOUT(i)
COMPARE
SYNDROME
INIT
PARITY
CORRECT
ECC-
Controller
ESTATE
CCLK
CCLK2
ERROR
LOCATION
ECC-
Controller
7 ECC-CODEC
ETRIG
VDD
IN
OUT
OUTB
CLK
CLKB
CLRB
ERROR
ECLK
RESET
24

FIG. 15

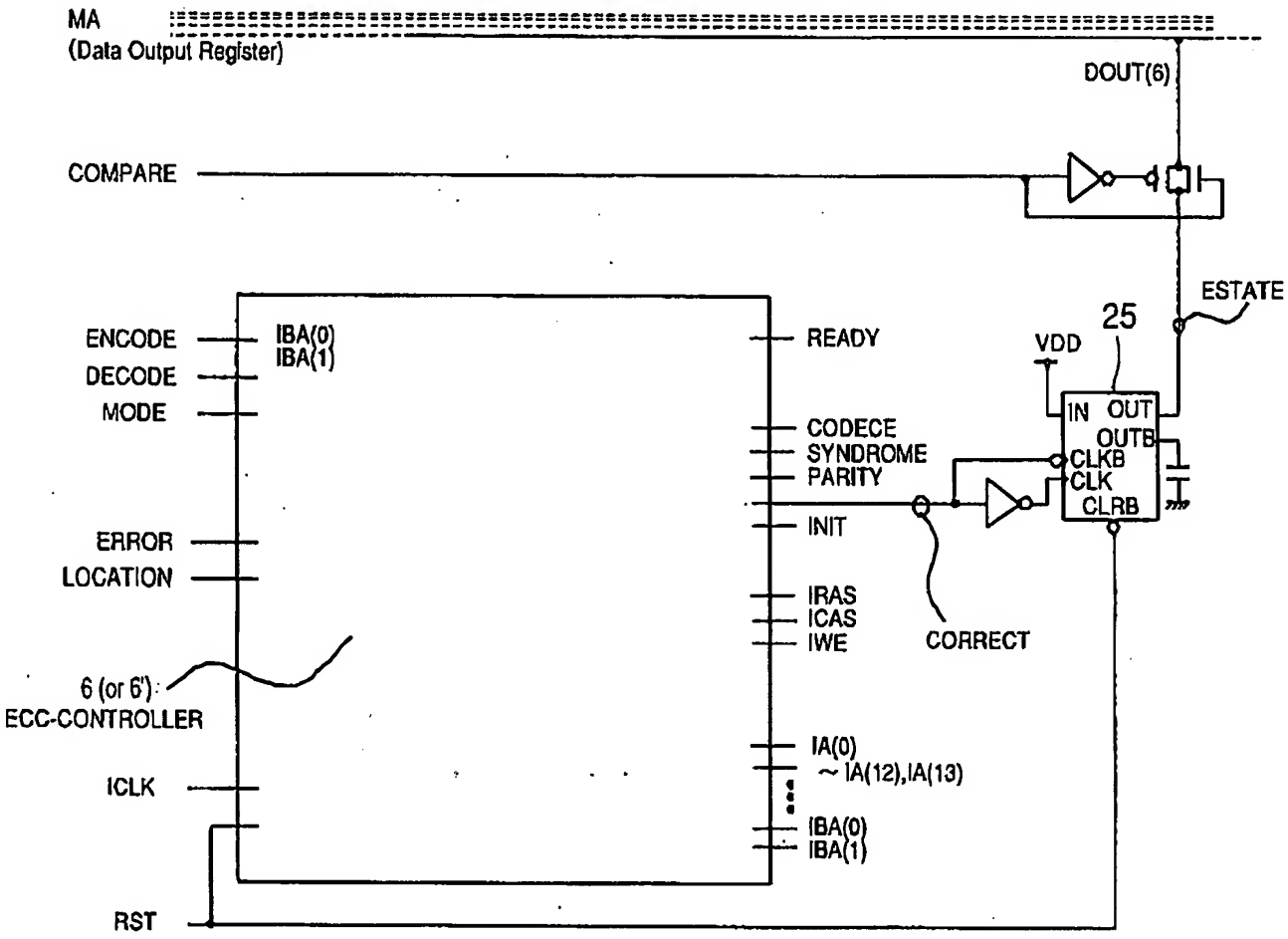

MA
(Data Output Register)
DOUT(6)
COMPARE
ESTATE
25
VDD
IN
OUT
OUTB
CLKB
CLK
CLRB
ENCODE
DECODE
MODE
IBA(0)
IBA(1)
READY
CODECE
SYNDROME
PARITY
INIT
IRAS
ICAS
IWE
CORRECT
ERROR
LOCATION
6 (or 6')
ECC-CONTROLLER
ICLK
IA(0)
~ IA(12),IA(13)
IBA(0)
IBA(1)
RST

FIG. 16

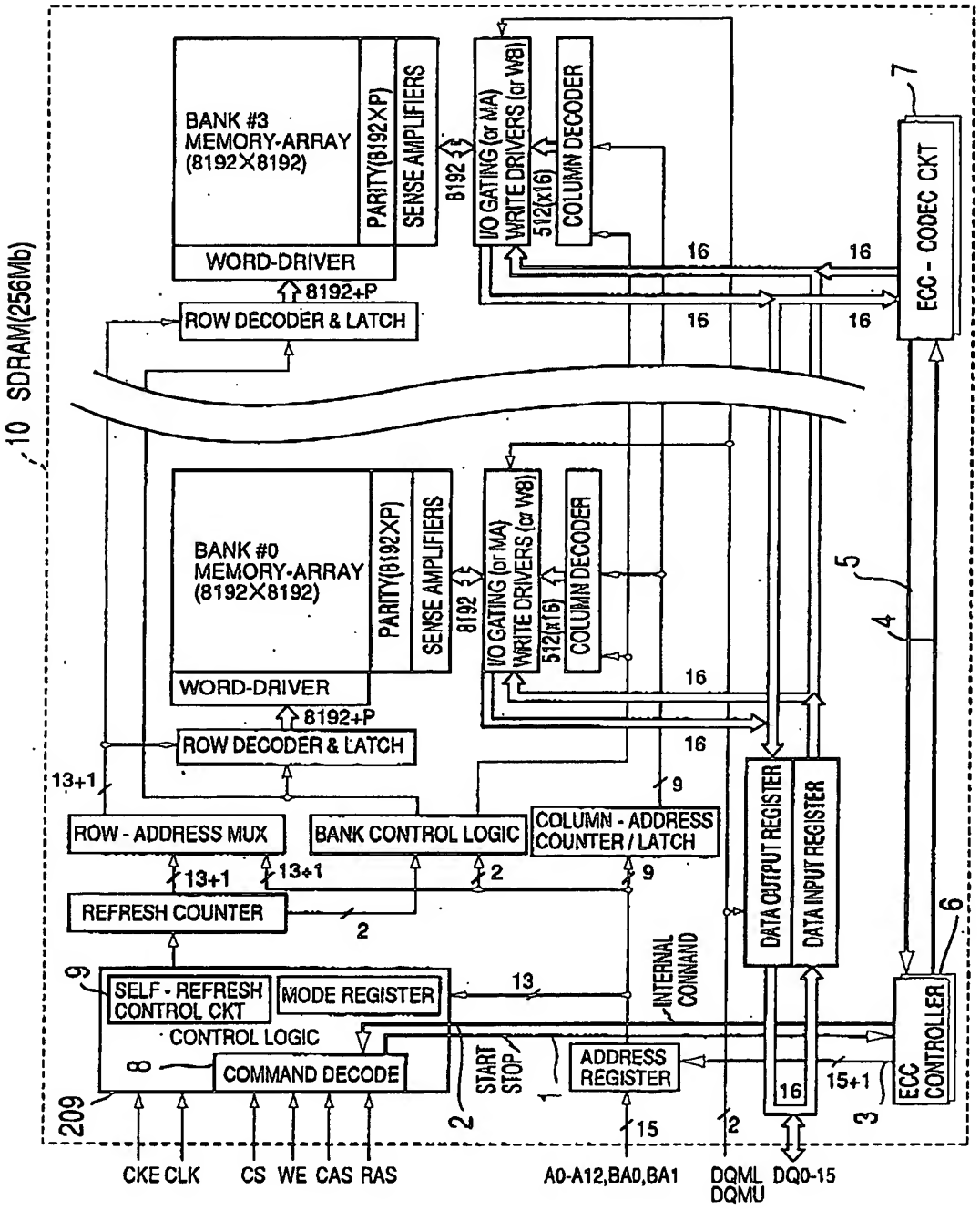

10 SDRAM(256Mb)
BANK #3 MEMORY-ARRAY (8192X8192)
PARITY(8192XP)
SENSE AMPLIFIERS
8192
I/O GATING (or MA) WRITE DRIVERS (or WB)
512(x16)
COLUMN DECODER
WORD-DRIVER
8192+P
ROW DECODER & LATCH
BANK #0 MEMORY-ARRAY (8192X8192)
ECC - CODEC CKT
7
5
4
16
13+1
9
ROW - ADDRESS MUX
BANK CONTROL LOGIC
COLUMN - ADDRESS COUNTER / LATCH
2
REFRESH COUNTER
DATA OUTPUT REGISTER
DATA INPUT REGISTER
6
SELF - REFRESH CONTROL CKT
MODE REGISTER
INTERNAL CONNAND
CONTROL LOGIC
COMMAND DECODE
START STOP
ADDRESS REGISTER
ECC CONTROLLER
15+1
3
209
CKE CLK
CS WE CAS RAS
A0-A12,BA0,BA1
DQML DQMU
DQ0-15

FIG. 17

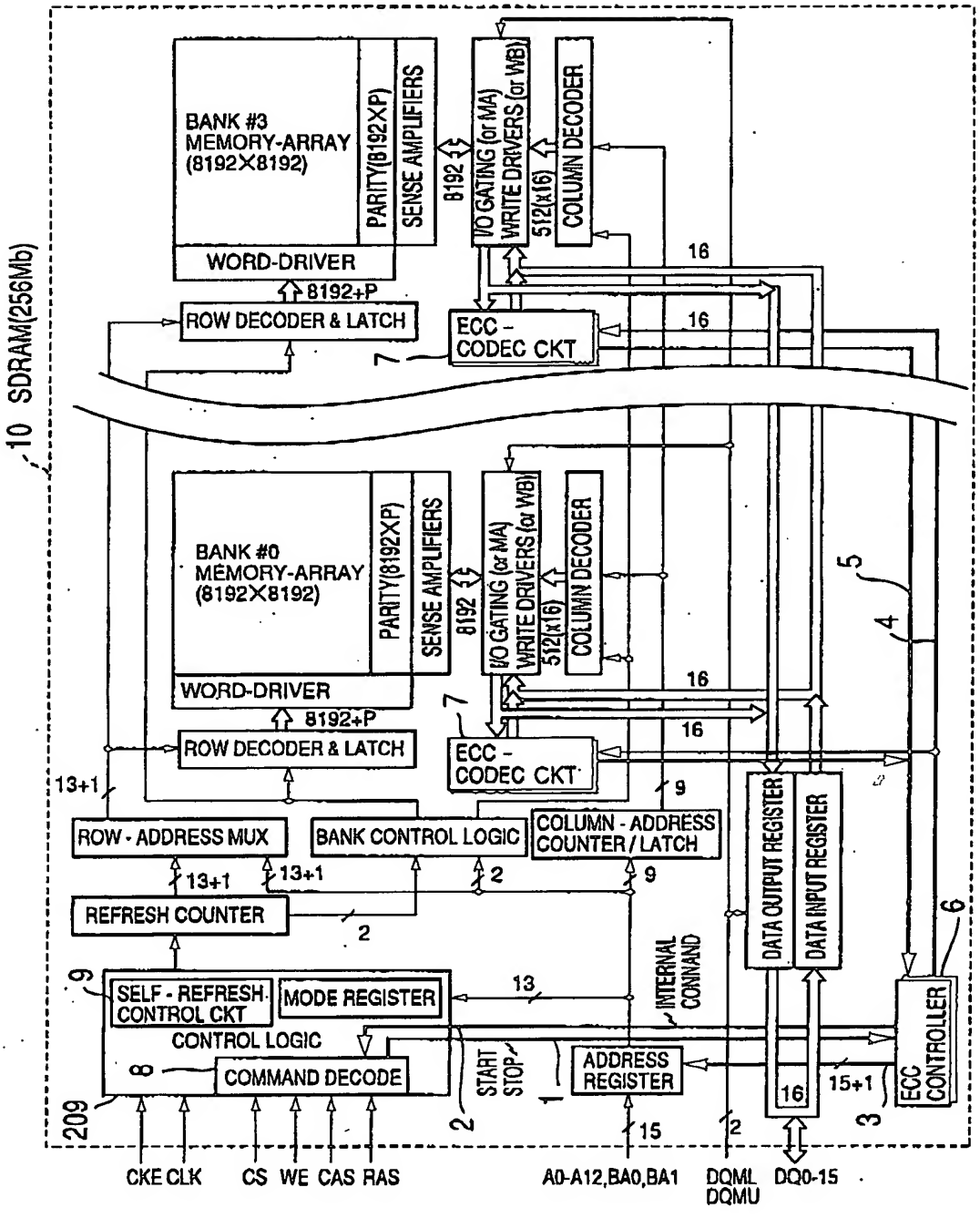
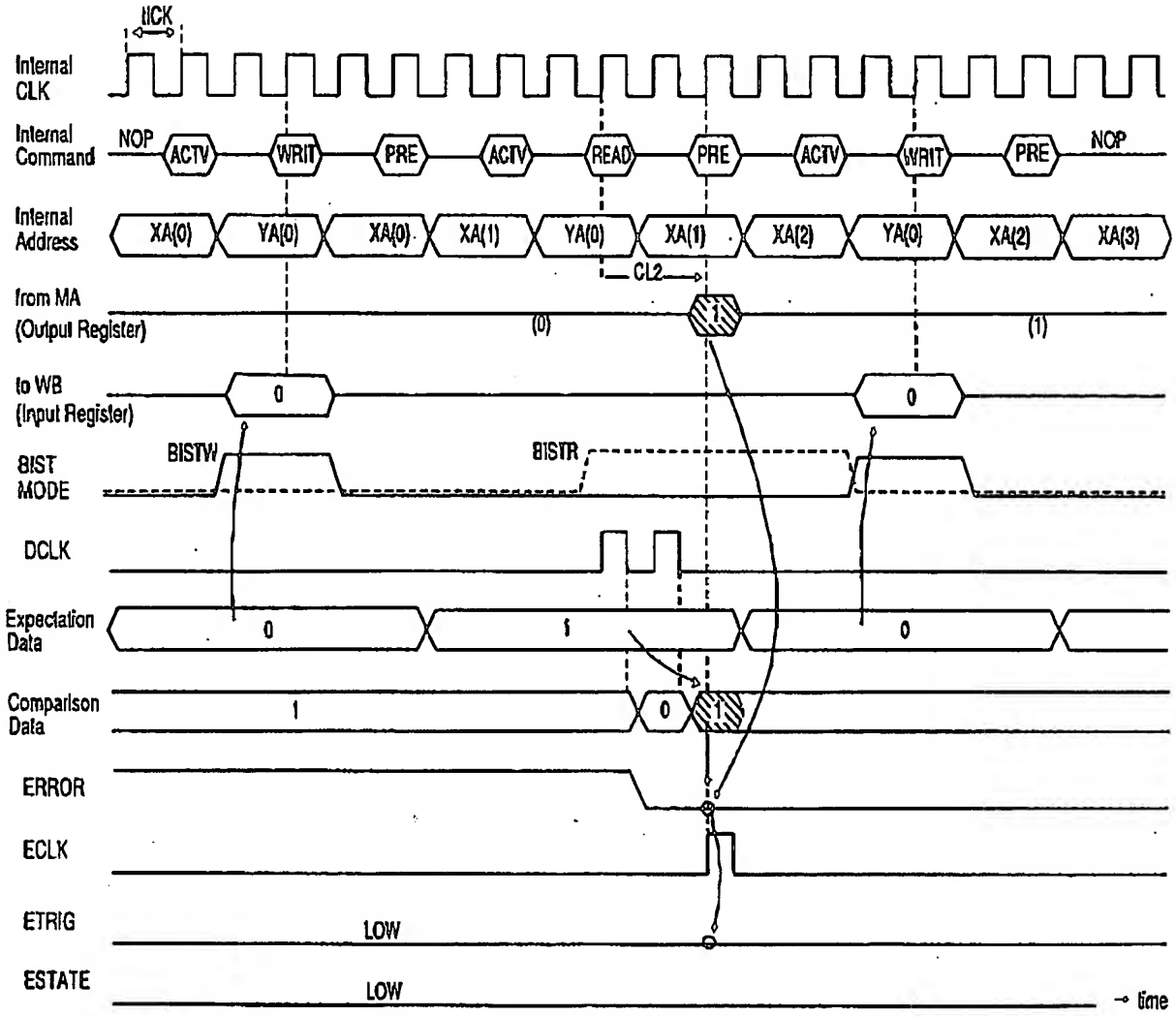
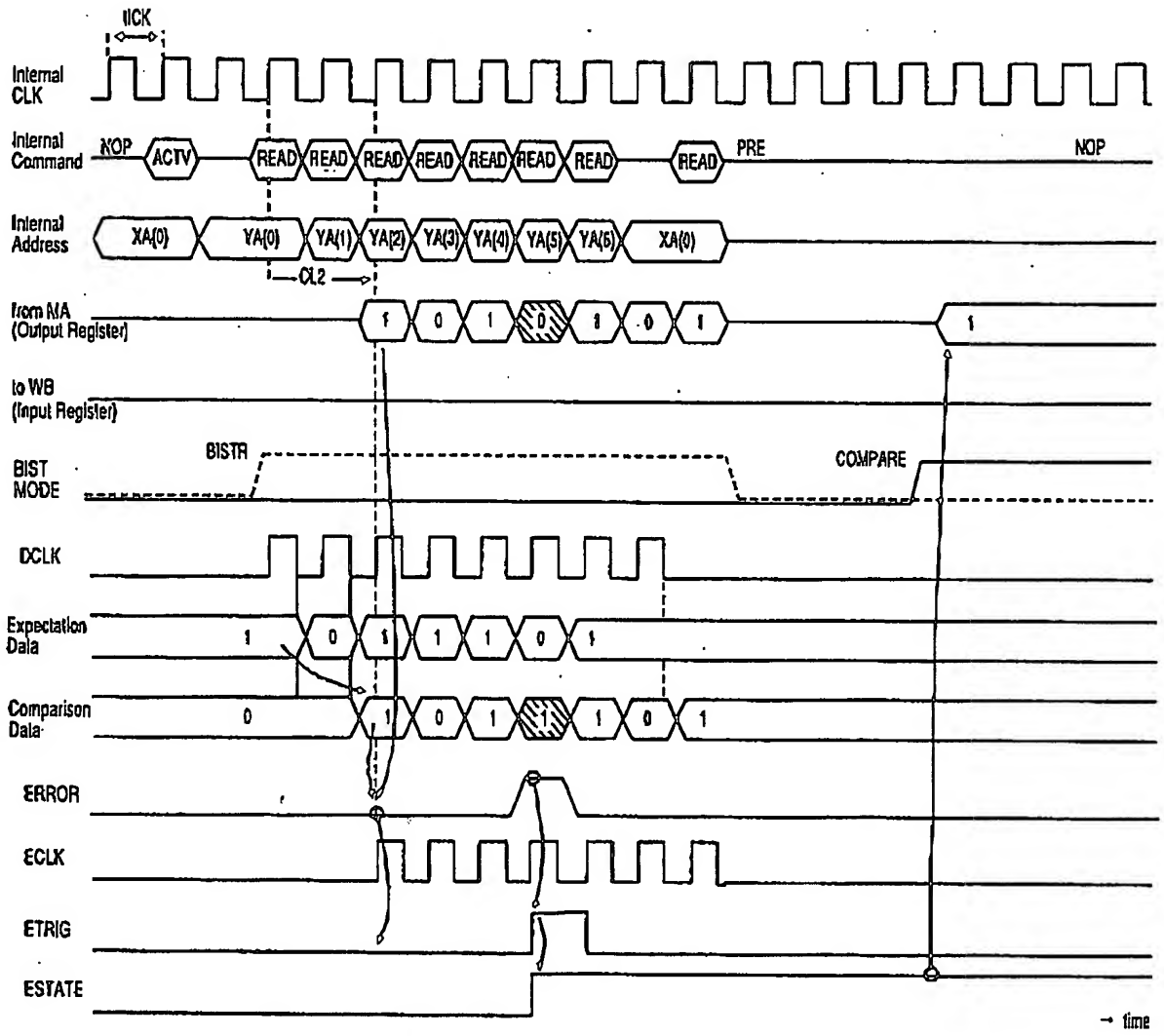

10 SDRAM(256Mb)
BANK #3
MEMORY-ARRAY
(8192X8192)
PARITY(8192XP)
SENSE AMPLIFIERS
8192
I/O GATING (or MA)
WRITE DRIVERS (or WB)
512(x16)
COLUMN DECODER
WORD-DRIVER
8192+P
ROW DECODER & LATCH
ECC -
CODEC CKT
16
7
BANK #0
MEMORY-ARRAY
(8192X8192)
13+1
ROW - ADDRESS MUX
BANK CONTROL LOGIC
COLUMN - ADDRESS
COUNTER / LATCH
9
2
REFRESH COUNTER
SELF - REFRESH
CONTROL CKT
MODE REGISTER
13
CONTROL LOGIC
COMMAND DECODE
8
209
START
STOP
1
INTERNAL
COMMAND
ADDRESS
REGISTER
15
DATA OUTPUT REGISTER
DATA INPUT REGISTER
ECC
CONTROLLER
15+1
3
6
5
4
CKE CLK
CS WE CAS RAS
A0-A12,BA0,BA1
DQML
DQMU
DQ0-15

FIG. 18




Example 1 of Self-Test Operation
(Burst Length 1, No Error)

FIG. 19




Example 2 of Self-Test Operation
(Burst Operation, Occurrence of Error, Reading of Result)

FIG. 20

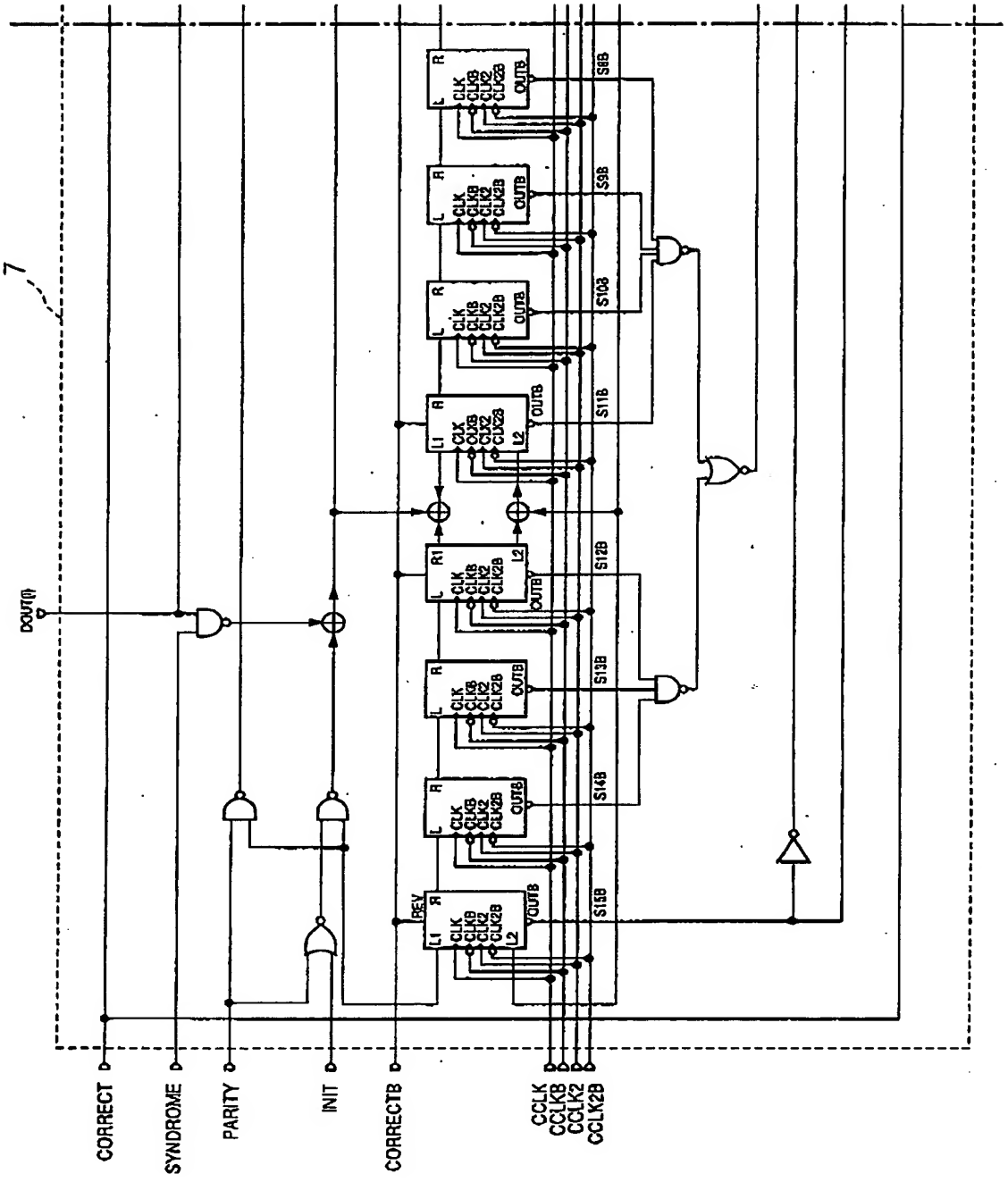

7
DOUT(i)
CORRECT
SYNDROME
PARITY
INIT
CORRECTB
CCLK
CCLKB
CCLK2
CCLK2B
DEV
S8B
S9B
S10B
S11B
S12B
S13B
S14B
S15B

FIG. 21

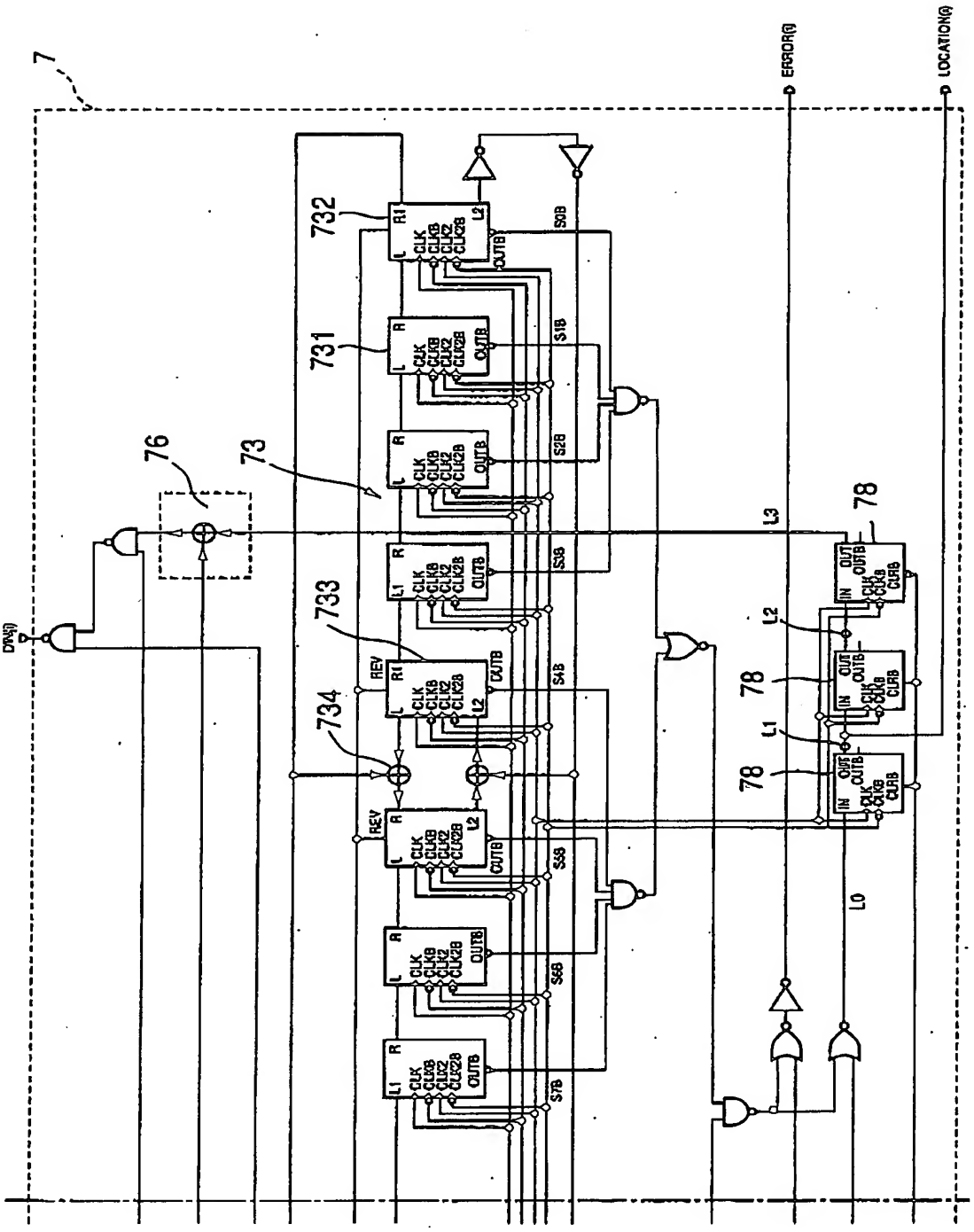

7
732
731
76
73
733
734
78
L3
L2
L1
L0
ERROR(0)
LOCATION(0)
DIN(0)
S0B
S1B
S2B
S3B
S4B
S5B
S6B
S7B

FIG. 22

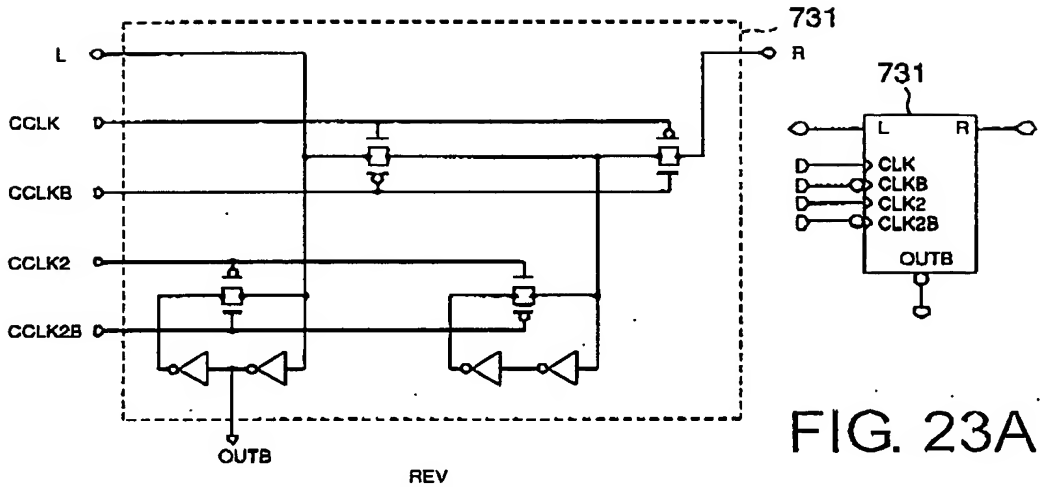



FIG. 23A

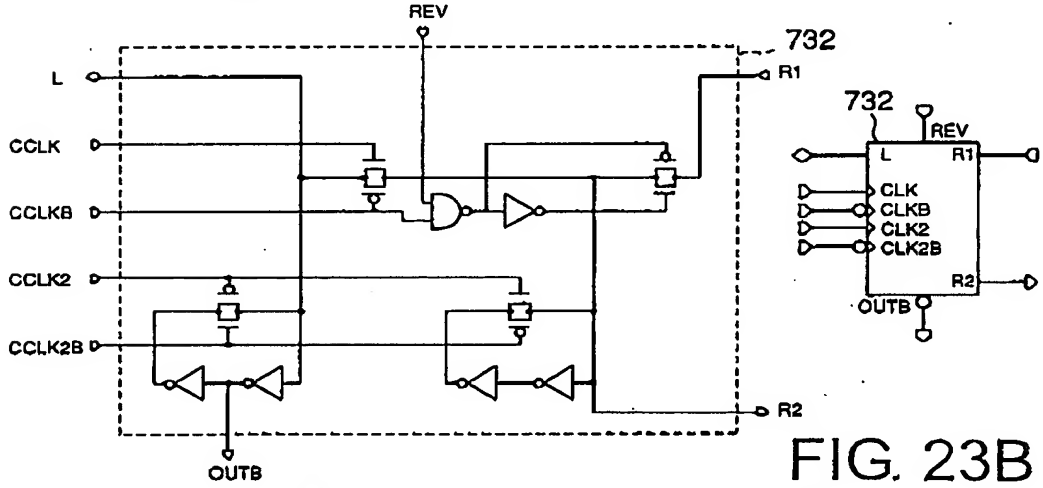



FIG. 23B

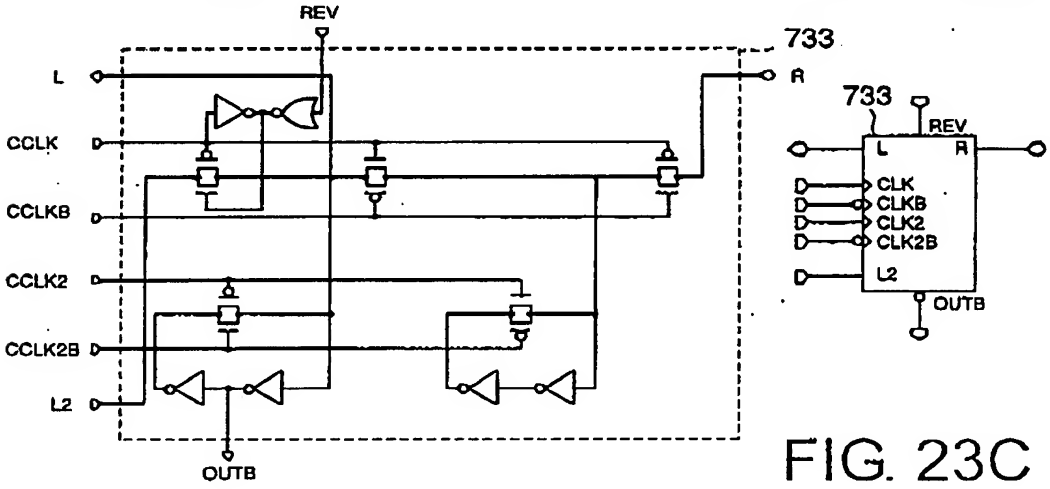



FIG. 23C

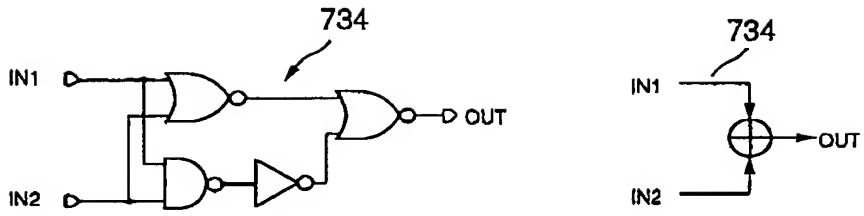

734
IN1
IN2
OUT
734
IN1
IN2
OUT

FIG. 24

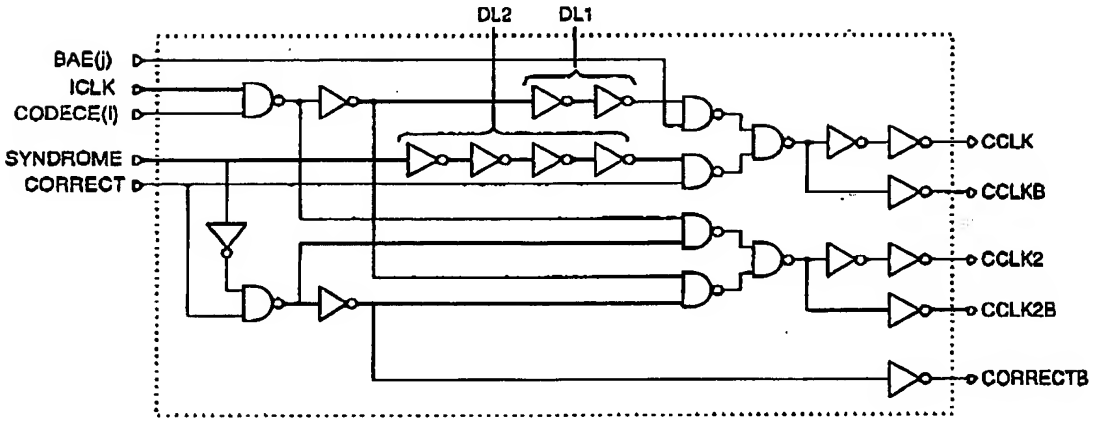
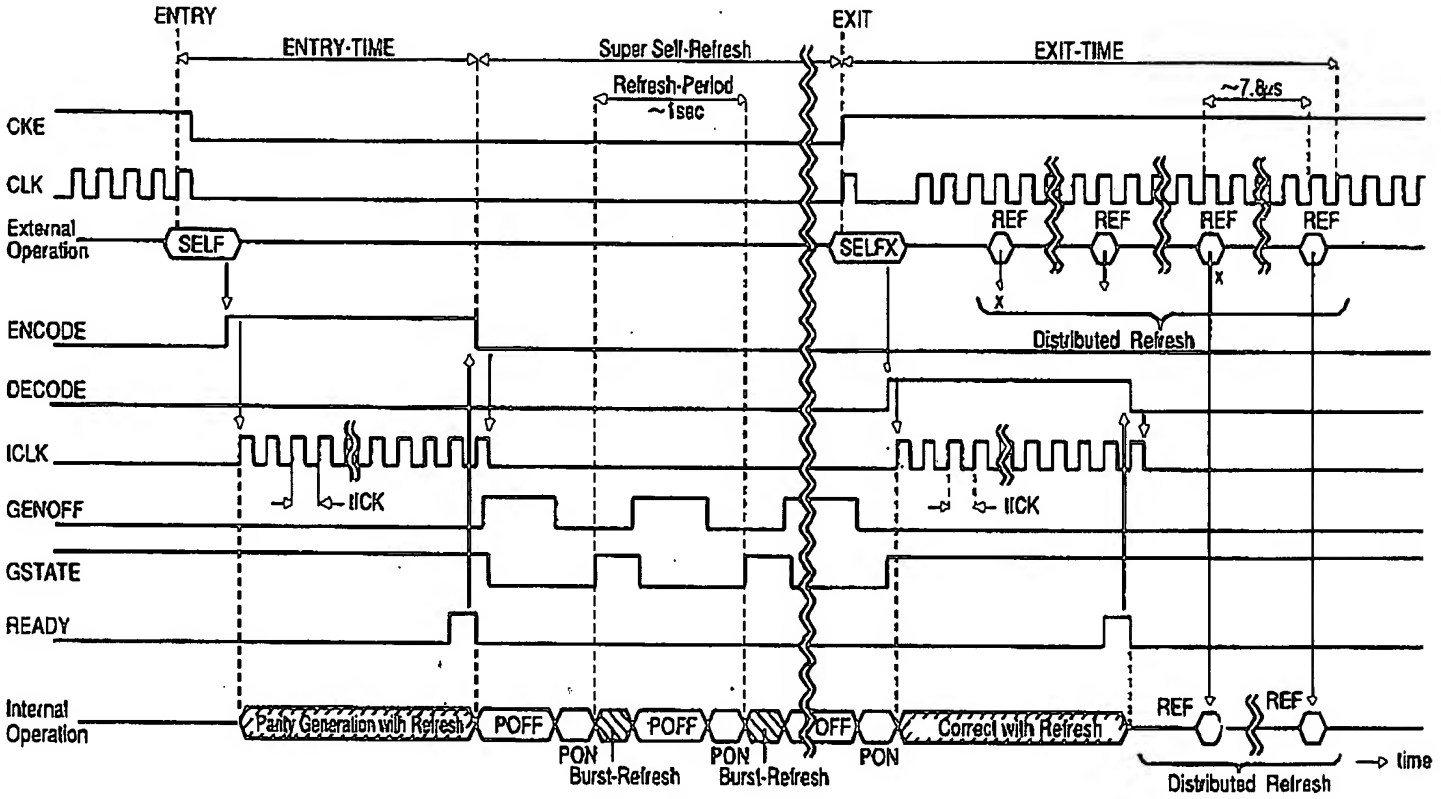

DL2
DL1
BAE(j)
ICLK
CODECE(I)
SYNDROME
CORRECT
CCLK
CCLKB
CCLK2
CCLK2B
CORRECTB

FIG. 25




Sequence of Super Self-Refresh Operation (Entry/Exit Scheme)

FIG. 26

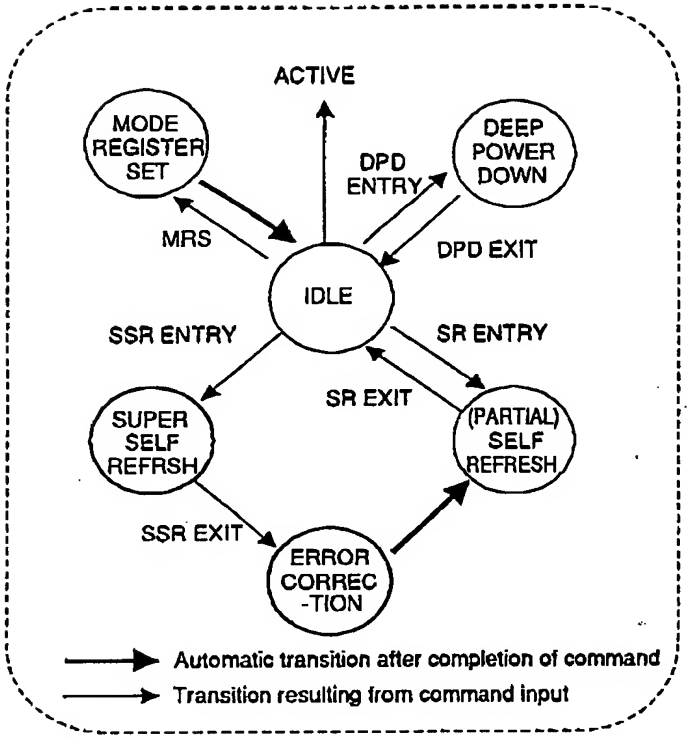

ACTIVE
MODE REGISTER SET
DEEP POWER DOWN
DPD ENTRY
MRS
DPD EXIT
IDLE
SSR ENTRY
SR ENTRY
SR EXIT
SUPER SELF REFRSH
(PARTIAL) SELF REFRESH
SSR EXIT
ERROR CORREC -TION
Automatic transition after completion of command
Transition resulting from command input

FIG. 27

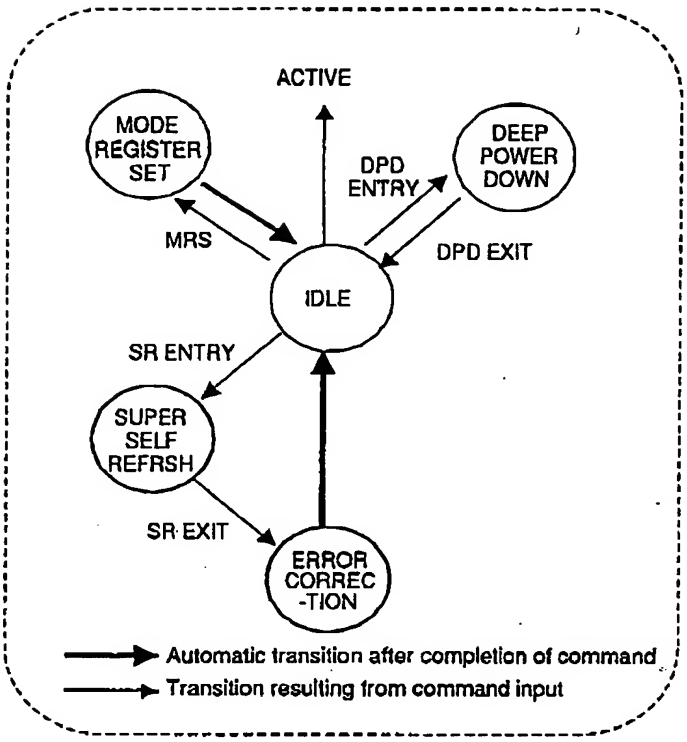

ACTIVE
MODE REGISTER SET
DEEP POWER DOWN
DPD ENTRY
MRS
DPD EXIT
IDLE
SR ENTRY
SUPER SELF REFRSH
SR EXIT
ERROR CORREC -TION
Automatic transition after completion of command
Transition resulting from command input

FIG. 28

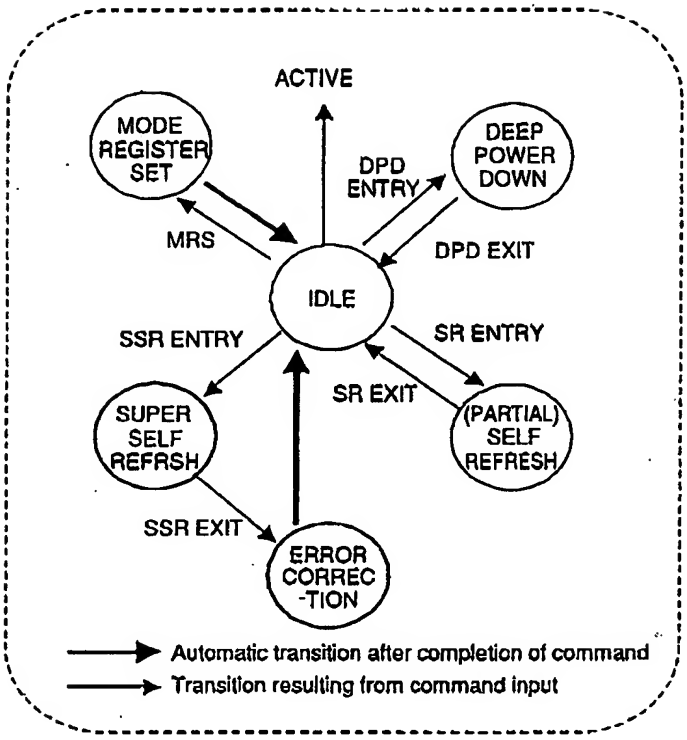

ACTIVE
MODE REGISTER SET
DEEP POWER DOWN
DPD ENTRY
MRS
DPD EXIT
IDLE
SSR ENTRY
SR ENTRY
SR EXIT
SUPER SELF REFRSH
(PARTIAL) SELF REFRESH
SSR EXIT
ERROR CORREC -TION
Automatic transition after completion of command
Transition resulting from command input

FIG. 29

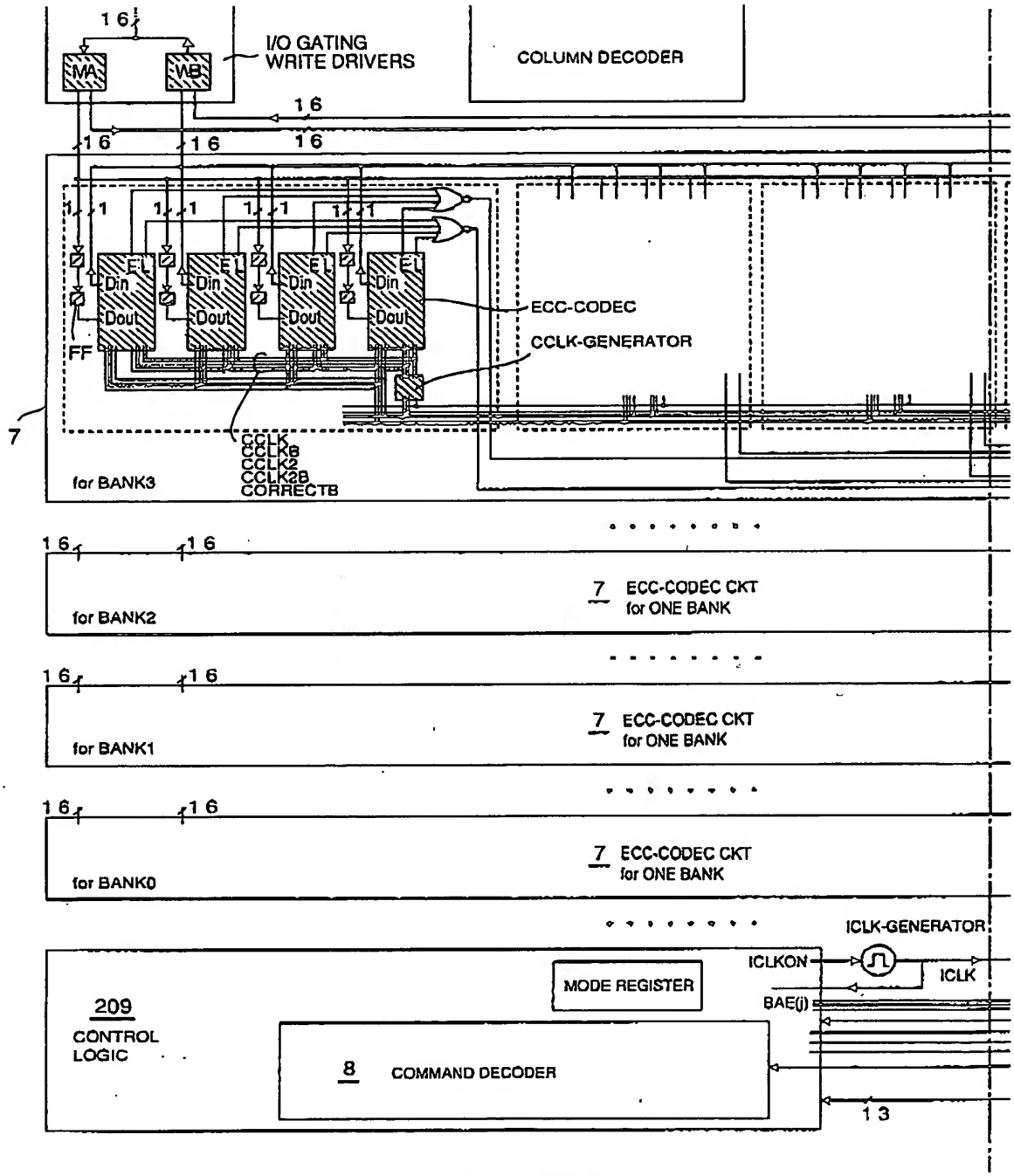

16
I/O GATING
WRITE DRIVERS
MA
MB
COLUMN DECODER
16
16
16
16
1
1
1
1
1
1
1
1
EL
EL
EL
EL
Din
Dout
Din
Dout
Din
Dout
Din
Dout
FF
ECC-CODEC
CCLK-GENERATOR
7
CCLK
CCLKB
CCLK2
CCLK2B
CORRECTB
for BANK3
16
16
7 ECC-CODEC CKT
for ONE BANK
for BANK2
16
16
7 ECC-CODEC CKT
for ONE BANK
for BANK1
16
16
7 ECC-CODEC CKT
for ONE BANK
for BANK0
ICLK-GENERATOR
ICLKON
ICLK
MODE REGISTER
BAE(j)
209
CONTROL
LOGIC
8
COMMAND DECODER
13

FIG. 30

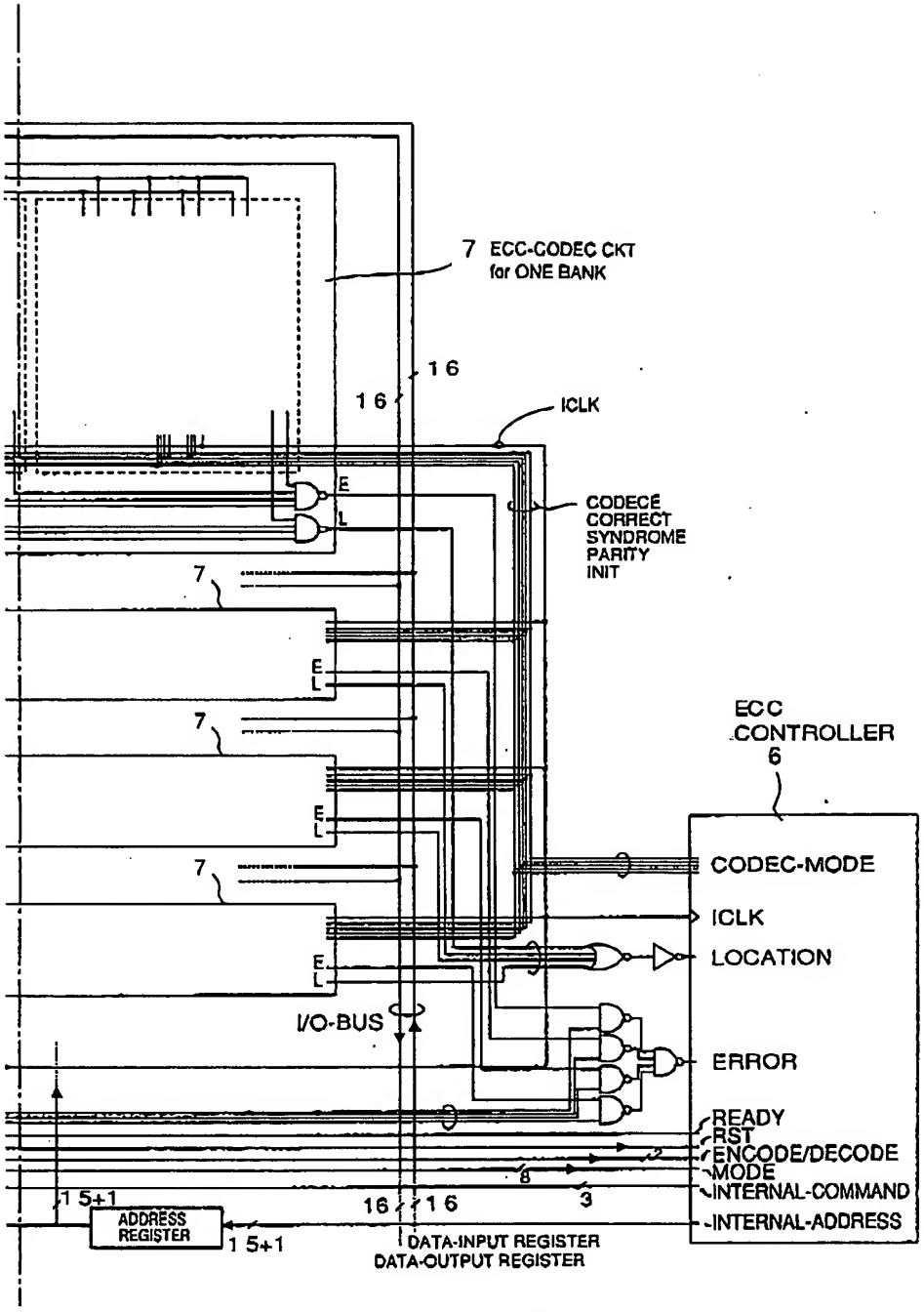

7 ECC-CODEC CKT for ONE BANK
16
16
ICLK
E
L
CODECE
CORRECT
SYNDROME
PARITY
INIT
7
E
L
7
E
L
7
E
L
ECC
CONTROLLER
6
CODEC-MODE
ICLK
LOCATION
I/O-BUS
ERROR
READY
RST
ENCODE/DECODE
MODE
INTERNAL-COMMAND
INTERNAL-ADDRESS
8
3
15+1
ADDRESS REGISTER
15+1
16
16
DATA-INPUT REGISTER
DATA-OUTPUT REGISTER

FIG. 31

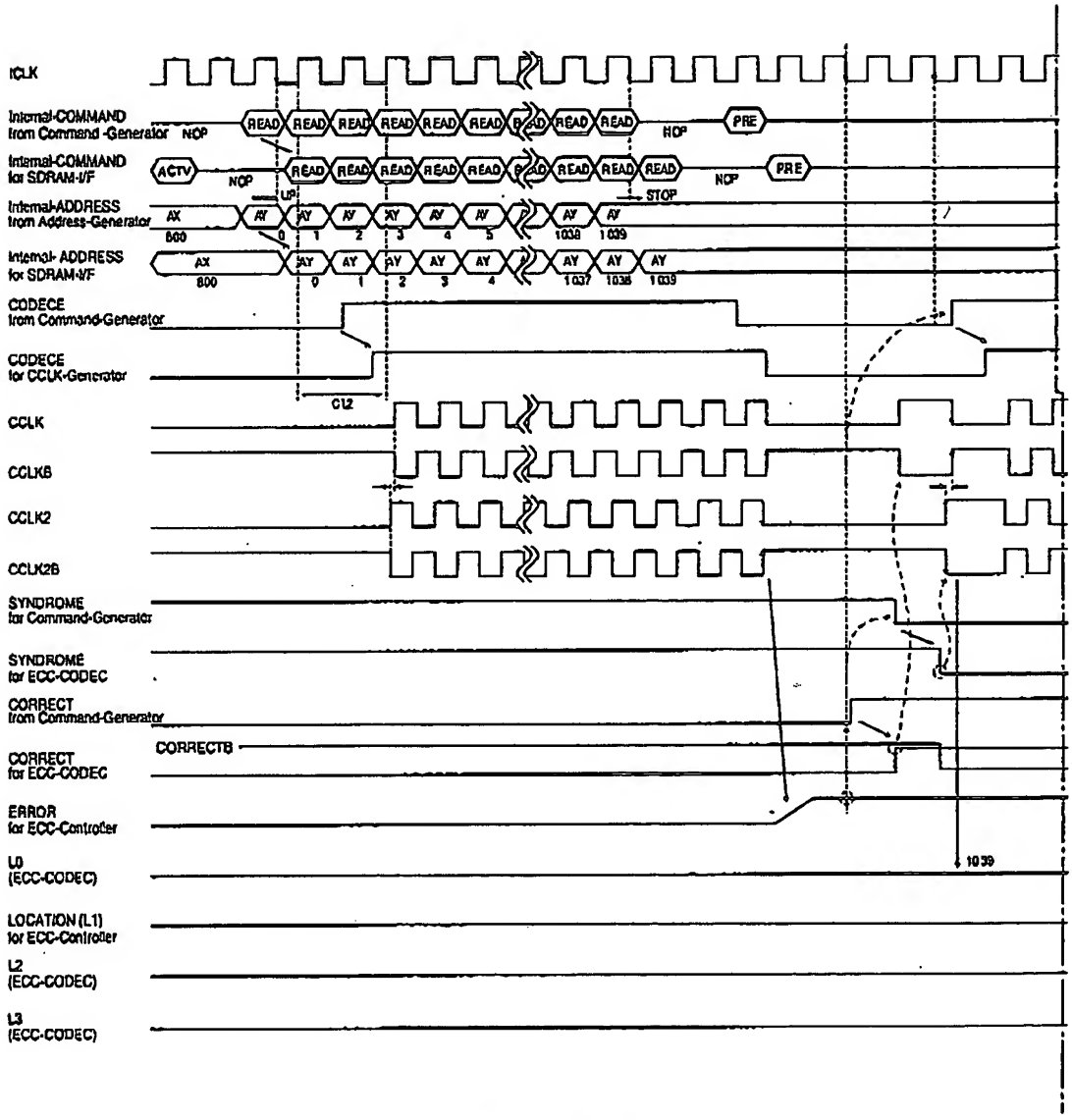

ICLK
Internal-COMMAND from Command -Generator
NOP
READ
HOP
PRE
Internal-COMMAND for SDRAM-I/F
ACTV
NOP
STOP
Internal-ADDRESS from Address-Generator
AX
AY
800
1038
1039
Internal- ADDRESS for SDRAM-I/F
1037
1038
1039
CODECE from Command-Generator
CODECE for CCLK-Generator
C12
CCLK
CCLKB
CCLK2
CCLK2B
SYNDROME for Command-Generator
SYNDROME for ECC-CODEC
CORRECT from Command-Generator
CORRECTB
CORRECT for ECC-CODEC
ERROR for ECC-Controller
L0 (ECC-CODEC)
1039
LOCATION (L1) for ECC-Controller
L2 (ECC-CODEC)
L3 (ECC-CODEC)

FIG. 32

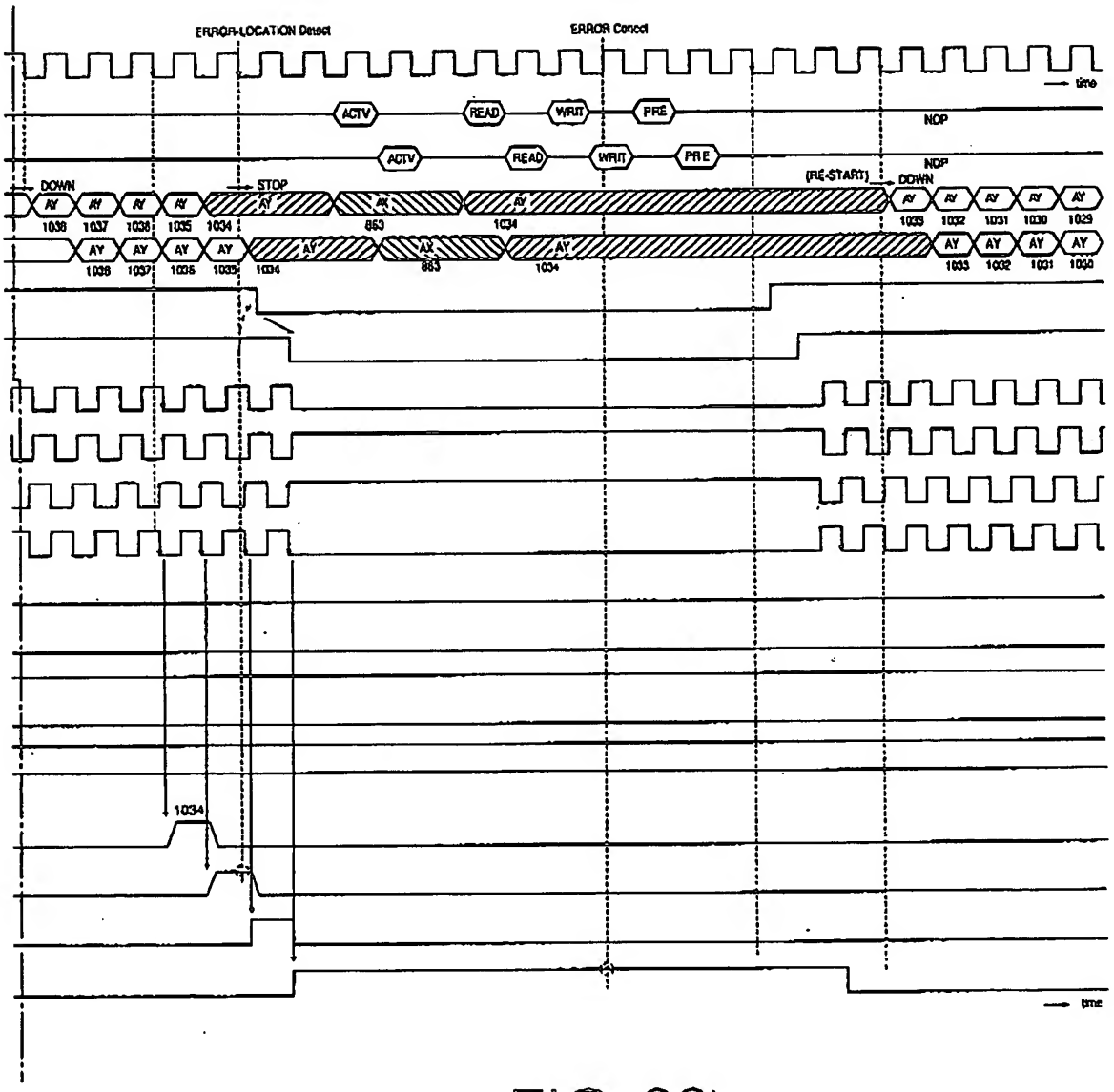

ERROR-LOCATION Detect
ERROR Cancel
time
ACTV
READ
WRIT
PRE
NOP
DOWN
STOP
(RE-START)
1034
time

FIG. 33